Hardware Link Level Emulator for System Level Simulations of WiMAX-like Systems

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Abstract: This paper describes the hardware link level emulator (HLLE) developed for hardware acceleration of the system level simulations of the WiMAX-like OFDM and OFDMA systems. The proposed architecture of the HLLE including transmit pipeline, channel emulator, receive pipeline and control blocks is presented. The performance characteristics of the developed HLLE are provided. It is demonstrated that application of the HLLE may increase the speed of simulations in about 200 times for link level simulations relatively to the software only simulations done using the PC. The application of the HLLE to the system level simulations is discussed. It is proposed that the HLLE may be used for the direct simulations of the individual links in the system level simulations rather than predicting performance of these links using PHY abstraction methodology.

Keywords: link level simulations, system level simulations, hardware emulator, hardware accelerator, WiMAX

1. Introduction

Simulations are an essential method in the design of the modern wireless communication systems. Typically the software models are developed for the transmitter, the propagation channel, the receiver, and some other phenomena that have to be taken into account. These software models are used to define the architecture of the communication system, predict different performance characteristics, and fine-tune various parameters before the actual system is implemented in hardware and may be tested over-the-air.

For the design of the large class of the communication systems it is sufficient to investigate by simulations only performance of the single transmit – receive communication pair (link). Such type of simulations is generally referred to as link level simulations.

However many modern wireless communication systems like cellular or broadband wireless access (e.g. WiMAX [1] and WiMAX-like) systems are required not only to provide the necessary link level performance characteristics but also to ensure the efficient simultaneous operation of multiple users in the complex interference-limited environment. To address these requirements during the design phase not only link level but also system level and network simulations have to be carried out. For the system level simulations, for example for WiMAX systems, typically the simulations of the multiple links operating simultaneously should be done. Such system level simulations are known to be cost and time consuming and obtaining results for these simulations requires significant computational resources.

To reduce the runtime and the cost associated with the simulation of the multiple communication links the physical layer (PHY) abstraction mechanism is usually used where the characteristics of the single link are predicted based on some channel quality indicator (CQI) which may be the channel mutual information, the instantaneous capacity, the signal-to-noise ratio (SNR) or the signal-to-interference-plus-noise ratio (SINR). Though different PHY abstraction methodologies are now widely applied in the system level and network simulations they still have several drawbacks. These drawbacks include the limited accuracy of the PHY abstraction models and significant increase of the PHY abstraction models complexity with the increase of the design complexity of the modern wireless MIMO-OFDM communication systems.

The alternative approach to performing the system level simulations with the reasonable runtime but without using the PHY abstraction techniques may be to keep the direct simulations of the multiple parallel links but to improve the speed of the link level simulations with the dedicated hardware accelerators. Such approach requires more design efforts at the first stage than software simulations but after implementation it will provide more accurate results within the shorter time frame.

The method of the hardware accelerated simulations is known in the literature and is used to perform in the dedicated hardware the reduced time simulations of the whole communication pipeline [2] or the most computationally intensive parts of it [3], [4]. Also the hardware accelerated simulations are extensively used for the performance evaluation of the error correction coding schemes at the very low bit error rate (BER) levels of 10^{-11} - 10^{-12} which practically can not be achieved with the software simulations [5], [6]. For most cases the implementation technology for the hardware accelerators is the Field Programmable Gate Arrays (FPGA) providing a massively parallel processing and reconfigurability.

In this paper the hardware link level emulator (HLLE) implementing the complete communication pipeline in the hardware for acceleration of the link level simulations is described. The proposed HLLE is realized using FPGA technology and allows several orders decrease of the simulation time for link level simulations relatively to the PC software simulations. Also the integration of the HLLE within the system level simulations is suggested.

The rest of the paper is organized as follows. Section 2 describes the architecture of the HLLE. Section 3 presents the performance characteristics of the developed HLLE. Section 4 explains the use of the HLLE for in the system level simulations. Section 5 concludes the paper.

2. Hardware Link Level Emulator Architecture

2.1. Architecture Overview

The HLLE is designed as a System-on-Chip (SoC) component that can be easily integrated to FPGA system to allow fast evaluation of wireless communication system characteristics. The high level diagram of developed Hardware Link Level Emulator (HLLE) is shown in Figure 1. The HLLE is composed of the three major signal processing blocks: transmit pipeline, channel emulator and receive pipeline and also of the control and interface blocks including bit error rate (BER) analyzer, interface to the system bus and register file. The further subsections describe the implementation of the individual blocks in more details.

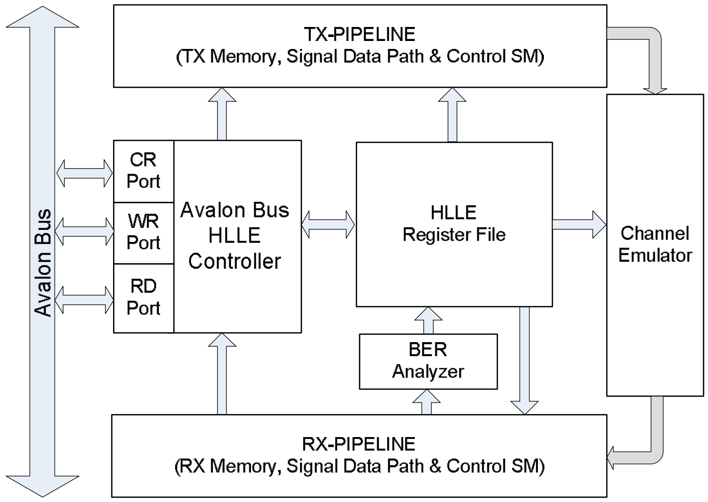

Figure 1. Architecture of hardware link level emulator

2.2. Transmit Pipeline

The transmit pipeline, channel emulator and receive pipeline constitute the signal processing part of the developed HLLE. The block diagram of the signal processing part of the HLLE is shown in Figure 2.

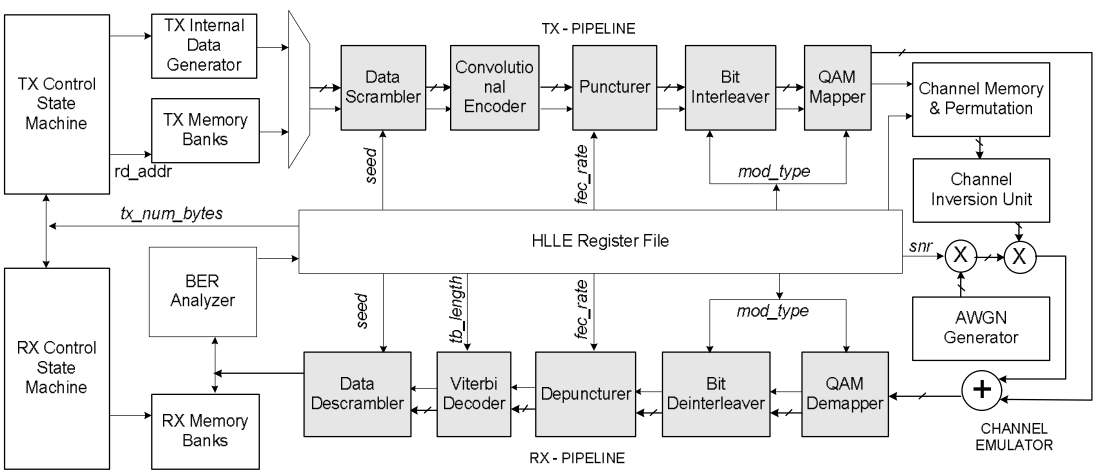

Figure 2. Signal processing blocks of HLLE

The *transmit pipeline* includes the basic blocks which are typical for transmit path of the OFDM communication system: scrambler to randomize data, forward error correction scheme based on convolutional encoder, puncturing scheme, bit interleaver and QAM mapper. The blocks are implemented mainly in accordance with IEEE 802.16 specification but are also extended to support the emulation of other systems. The output of the transmit pipeline are QAM modulated symbols. Four modulation types are supported: BPSK, QPSK, 16-QAM and 64-QAM. The output signals are organized in blocks of 48 symbols. Such division by blocks allows emulation of OFDMA sub-channels with different types of tone permutations by supplying corresponding channel coefficients in the channel emulator block.

2.3. *Channel Emulator*

The wireless communication system usually experiences the frequency selective linear distortion due to multi-path propagation and the impact of the additive white Gaussian noise (AWGN) due to the thermal noise of the receive RF chains. These are the main effects that have to be captured in the simulations of the wireless communication systems. For signal processing acceleration the HLLE was designed so that to be able to take these effects into account with the help of the specific channel emulation scheme. The channel emulation scheme implements dedicated signal processing path differently to the real-world system but providing equivalent performance from the simulations point of view. The first assumption (simplification) relatively to the real-world system used in the HLLE is that the channel emulation is done in the frequency domain rather than in the time domain. The calculation of the frequency domain channel transfer function is done offline before the start of the HLLE simulations. The second assumption is the following. The real-world OFDM or OFDMA system employs equalizer to align the power of the signals transmitted at different subcarriers to perform their demodulation. The equalization leads to the appearing of the frequency selectivity of the additive Gaussian noise introduced at the receiver. The proposed channel emulation scheme does not perform frequency selective distortion of the transmitted symbols and then its equalization after introduction of the AWGN noise. Instead the appropriately frequency distorted additive Gaussian noise is introduced by the channel emulation scheme.

The proposed approach of the channel emulation applies equally to the different space-time transmission scheme but in this case the conversion of the MIMO channel to several equivalent post-processing SISO channels has to be performed before the start of the simulations.

Additionally the channel emulator block allows application of the different permutation schemes by interchanging the channel coefficients for different subcarriers to allow the emulation of the OFDMA systems.

The high-performance white gaussian noise generator based on Box-Muller method [7] was designed for the HLLE using architecture similar to one proposed in [8]. The designed generator has periodicity of 10^{15} samples and simultaneously produces two accurate 16 bit noise I and Q samples that precisely model the true Gaussian PDF up to 8.2σ .

2.4. *Receive Pipeline*

The *receive pipeline* accepts transmitted frequency domain signal samples with introduced frequency selective additive Gaussian noise. The operations performed by the receiver pipeline are reciprocal to the operations done by the transmit pipeline and include demapping, deinterleaving, depuncturing, decoding and descrambling. The estimated bit sequence is then compared with transmitted bits and error calculation is done in the BER analyzer module.

2.5. *Control and Interface Blocks of HLLE*

The control and interface blocks of the HLLE are composed of the Avalon Bus HLLE controller and HLLE Register File. The Avalon SoC bus from Altera is used because the designed HLLE was targeted mainly for implementation with the Altera Stratix FPGA technology.

Custom Avalon HLLE controller with three slave configuration ports is used for configuration and control of HLLE. This controller provides to external devices the access to internal memory banks and HLLE Register File.

HLLE Register File is designed to keep configuration parameters and control operation of HLLE during simulation cycle. The main parameters stored in this register file are the length of packet to be transmitted, its modulation and code rate, level of additive white Gaussian noise, number of channel coefficients, number of parallel spatial channels to be processed. It also control the BER analyzer during the simulations.

3. Performance Characteristics of HLLE

3.1. Simulation Accuracy of HLLE

In order to test the performance of the developed HLLE in terms of bit error rate (BER) accuracy, the simulation results were obtained with the HLLE and compared against the reference floating point software model of the communication link. The simulations were performed for additive white gaussian noise (AWGN) channel model using different modulation and coding schemes (MCSs) – QPSK ½, 16-QAM ¾ and 64-QAM 2/3. The BER results for each SNR point were simulated by averaging over 10000 frames with each frame having 1 KB length. The obtained BER results are shown in Figure 3.

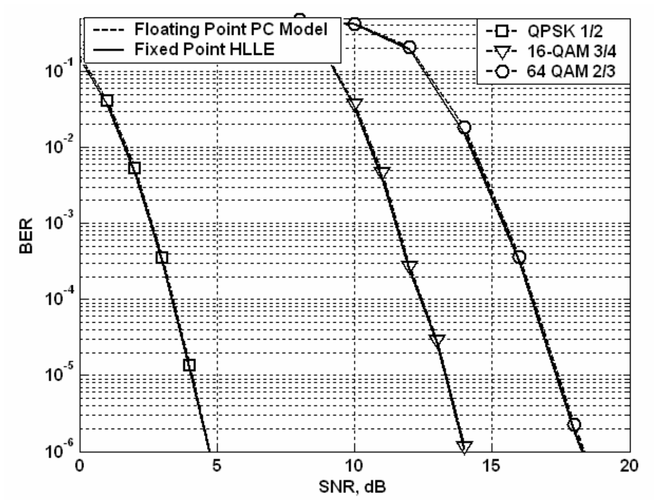

Figure 3. BER results for HLLE and reference floating point model in AWGN channel

It can be seen that for all simulated points the HLLE results match very well the results obtained with the reference floating model. The deviation between two simulation methods is less than 0.1 dB. The typical accuracy of the PHY abstraction models is known to be about 1 dB. So the application of the HLLE may significantly improve the accuracy of the system level simulation results.

3.2. Characteristics of FPGA Implementation of HLLE

The characteristics of the HLLE implementations were analyzed for Altera Sratix, Stratix II and Stratix III FPGA families. Table 1 shows the results of the logical synthesis obtained for these devices.

It can be seen from the Table 1 that the HLLE may provide throughput from 60 to 140 Mbit/s and requires from 15K to 17K of equivalent logic elements depending on the FPGA implementation technology.

Table 1. Characteristics of FPGA Implementation of HLLE

Synthesis results	Stratix I	Stratix II	Stratix III
Max clock frequency, MHz	60	140	132
Max throughput, Mbps	60	140	132
Number of equivalent logic elements (LEs) occupied by HLLE	15300	17000	17260
Memory size required for HLLE, Kbits	214	214	401
Number of DSP blocks used by HLLE	19	19	19

3.3. Comparison of simulation speed between HLLE and software simulator

To estimate the increase of the simulation speed provided by the HLLE relatively to the software simulations the runtime required for each method was measured for link level simulations of 1000 data packets with the packet length equal to 1000 bytes. Five different MCSs were considered. The PC with Xeon 3.4 GHz CPU and 2.0 GB of RAM was used to perform the software simulations and the HLLE was run at the Altera Stratix II FPGA on the DSP Development kit, Stratix II Professional Edition [9] at 100 MHz clock rate. The results of the comparison are presented in Table 2.

Table 2. Comparison of simulation speed between HLLE and software simulator

MCS	Software simulator		HLLE		Simulation speed increase, times
	Time, s	Throughput, Mbps	Time, s	Throughput, Mbps	
BPSK ½	71.0	0.11	0.33	24.24	215.2
QPSK ½	50.0	0.16	0.25	32.00	200.0
QPSK ¾	42.3	0.19	0.18	44.44	235.0
16 QAM ½	46.0	0.17	0.21	38.10	219.0
16 QAM ¾	38.0	0.21	0.15	53.33	253.3

As it follows from the Table 2 the HLLE provides on average from 200 to 250 increase of the simulation speed relatively to the software simulator run on the reference platform.

4. HLLE Integration with System Level Simulator

As it is outlined in the introduction of this paper the system level simulations of WiMAX and WiMAX-like systems are considered as a main application of the developed HLLE.

The general block diagram of the system level simulations is shown in Figure 4. The system level simulations are performed by iterating over multiple system realizations. Each realization is generated according to some scenario including downlink or uplink modes, number of BS and SS, their geographical distribution, shadowing and channel model parameters, etc. Then the performance parameters for the individual system realization are calculated. At the end of the simulation the statistical processing of the obtained results for multiple system realizations is performed to estimate the system performance characteristics, like average spectral efficiency, outage probability and others.

The steps performed by the system level simulator for evaluation of the performance of the single system realizations include [9] (steps 2-6 in Figure 4): generation of the multiple base stations (BS) and subscriber stations (SS) within the hexagonal grid of cells, generation of channel realizations between all SS and BS, assigning SS to BS, scheduling of time-frequency resources of different SS for all cells, calculation of SINR values for each time-frequency slot of each SS in the central cell, evaluation of the performance of the individual links and performing the statistical processing of the performance characteristics obtained for different users within the current system realization.

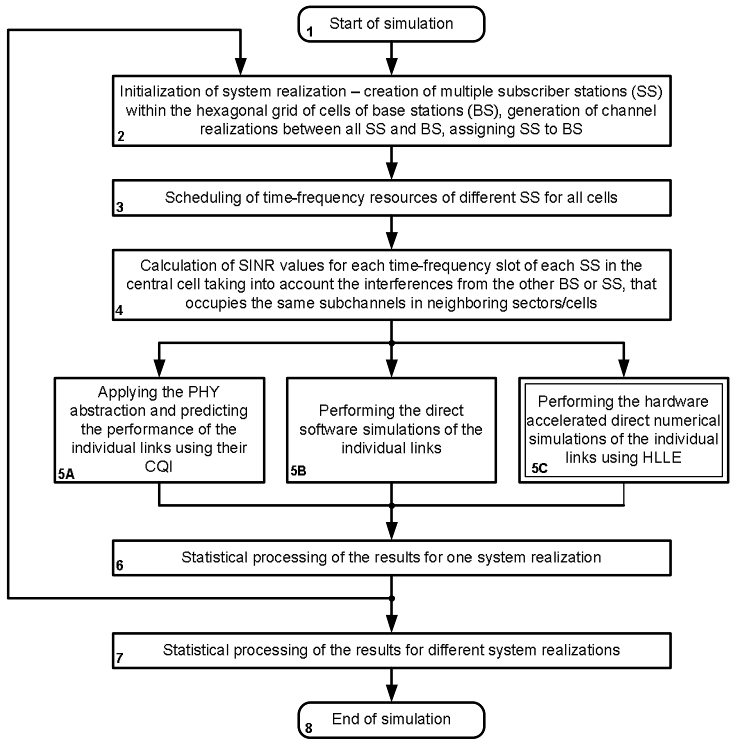

Figure 4. Block diagram of system level simulations

The performance evaluation of the individual communication links (step 5 in Figure 4) can be done differently. Three possibilities include predicting performance using CQI (step 5A), performing direct numerical simulations using software link level simulator (step 5B) and using HLLE to carry out direct numerical simulations accelerated in hardware (step 5C).

The advantage of applying PHY abstraction methodology relatively to the case of using direct link level software simulations is the reduction of the simulations runtime. The disadvantage of using PHY abstraction relatively to both other methods is the necessity to develop and verify the PHY abstraction methodology providing the required accuracy which may be a complicated task and consume significant design resources. The method of direct numerical software simulations does not require additional design effort for neither developing the PHY abstraction nor performing the hardware design. But the runtime of the direct numerical simulations may become prohibitively large even if the high performance distributed computational clusters are used for this task. The use of the HLLE has advantages of both other approaches of small simulation runtime and not requiring the PHY abstraction methodology development but the obvious drawback of the HLLE-based approach is the higher design effort required to implement the functionality of the link level simulator in hardware.

Taking into account all the above given considerations for three possible methods of performing the system level simulations it is believed that the proposed HLLE-based approach has a good perspective to become widely accepted for the performance evaluation at the system level of the modern multi-user broadband wireless communication systems.

5. Conclusions

In this paper the hardware link level emulator (HLLE) is proposed which can be used for the accelerated link level simulations of the communication links of the modern OFDM or OFDMA communication systems. The architecture of the HLLE, including the hardware implementation of the OFDM/OFDMA simulation pipeline is described. The obtained implementation characteristics of the developed HLLE are presented. It is demonstrated that application of the HLLE may improve the speed of link level simulations in about 200 times relatively to the software only simulations.

The proposed HLLE has a good potential for application in the system level simulations of the WiMAX and WiMAX-like systems. The facts advocating the use of the HLLE are the increasing complexity of the multi-user communication systems requiring obtaining of a large number of the simulation results for the system level rather than the link level parameters within the reasonable time. The other important tendency is the increase of the PHY abstraction complexity and the associate design effort for developing it to address the constantly increasing complexity of the multi-user space-time signal processing algorithms employed by the modern wireless communication systems.

The further work on extending the concept of the HLLE application to the system level simulations will include the actual integration of the HLLE to the system level simulator and performing comparison of its performance relatively to the PHY abstraction based and direct software simulations approaches.

6. Acknowledgement

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