A 32-Ch. Bidirectional Neural/EMG Interface with on-Chip Spike Detection for Sensorimotor Feedback

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OVERVIEW

- Implantable neural stimulation and recording platform, 0.35 μm HV tech. node
- 32 bidirectional channels - 32 recording front ends and 1 multiplexed stimulator
- 16 kHz sampling using 1-4 multiplexing with 8 10-bit ADCs
- 225 to 4725 programmable gain recording chain
- On-chip spike detection and spike window transmission
- 9.25 V compliance and up to 315 μA output current for stimulation
- Electrode monitoring and shorting for balancing residual charge
- Programmable stimulation pulse train using custom stimulation scheduler
- Suitable for chronic use

Aims and Objectives

- Implantation in the rat animal model presents design constraints on size and power.
- To design a system suitable for chronic use, wireless transfer of power and data is required.
- The system is designed for low-power operation with reduced data rates.
- The implant size cannot exceed 1 cm² so encapsulation requires the chip to fit within a 4 by 4 mm square.
- Useability with high-impedance penetrating electrodes requires high voltage compliance.
- Protecting neural recording amplifier input pairs from overvoltage during stimulation requires HV MOSFETs or diodes in the signal path.

Front-End Circuits

- HV MOSFETS and diodes protect the sensitive low-voltage analog recording.
- One method is used per channel to allow determination of the best solution experimentally.
- HV cascading transistors yield high output resistance and resistors drive down VDD, improving voltage compliance.
- Shutdown transistors save system power when not stimulating.

Spike Detection

- Spike window transfer enables additional power efficiency and low data rates.
- Raw data still accessible.

KEY RESULTS

- Gate overvoltage protection using diodes or HV MOSFETs.
- Low-power @ 23 μW per recording channel.
- 0.081 INL with 6-bit DAC.
- 0.02% charge imbalance for 5 nC stimulation charge.

REFERENCES