Scalable Neural Recording Interface with Real-time Spike Sorting

NGNI-V1 Platform
OVERVIEW

Spike Sorting On-Node and Real-Time

Spike Sorting is the process of deinterleaving a recorded neural signal in order to determine the firing patterns of individual neurons from the aggregate spike stream.

The NGNI platform is an end-to-end solution for on-node, real-time spike sorting. By using a compact, onboard (template based) spike sorting engine, together with offline training (WaveClus-based), a low power real-time solution is achievable.

The main components of the NGNI-v1 module are an Intan RHD2132 neural amplifier and a low power Igloo FPGA. The Intan RHD2132 contains 32 low noise amplifiers and bandpass filters multiplexed into a single 16-bit ADC for neural signal filtering, amplification & digitisation. The low power Igloo FPGA performs spike sorting and communication. It also includes a standard pitch header (for connection to electrodes) and a micro HDMI connector for digital communication (and if desired external power). If used in conjunction with the NGNI USBridge motherboards this power can safely be sourced from USB and can allow for limited scalability (160 channels).

The system operates in a two stage process that leverages the high performance unsupervised spike train clustering and deinterleaving capability of a proprietary WaveClus implementation. In the first stage the NGNI-v1 is configured to send raw data to a computer for offline analysis with WaveClus. The generated templates (up to 4 per channel) are then uploaded to the NGNI-v1 which implements a computationally efficient algorithm to perform real-time spike sorting. The spike sorted data is transmitted via the NGNI USBridge (over SPI and then USB) to a PC. A GUI is provided for data visualisation and system configuration.

FEATURES

- 32-channel neural recording/streaming
- On-node, real-time template-based spike sorting
- Proprietary template building engine (based on WaveClus)
- Onboard template memory, 18.4kbit (4 templates per channel)
- Low latency (0.3ms) SPI output
- Low output datarate for wireless communication

APPLICATIONS

- Signal acquisition systems for electrophysiology
- Large-scale recording applications (multi-probe, multi-channel)
- Realtime brain machine interface applications
- Closed loop low-latency biofeedback
This is the first compact design targeted at in-vivo application. Size and weight have been reduced while extra functionality has been included such as:

- An extra SPI link enables MCU expansion and standalone operation or wireless connection.
- Simultaneous matching events and raw signal output
- CMOS outputs for matching event on selected templates

**ELECTRICAL SPECIFICATION**

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<table>
<thead>
<tr>
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<tbody>
<tr>
<td><strong>Power supply</strong></td>
<td>3.13-5.5 V</td>
<td><strong>CMRR</strong></td>
</tr>
<tr>
<td><strong>Amplifier differential gain</strong></td>
<td>192</td>
<td><strong>PSRR</strong></td>
</tr>
<tr>
<td><strong>Sampling rate</strong></td>
<td>15 kHz</td>
<td><strong>THD</strong></td>
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<tr>
<td><strong>(1kHz, 4mVpp, 0.1-10kHz)</strong></td>
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<td><strong>ADC resolution</strong></td>
<td>9-bit</td>
<td><strong>Amplifier crosstalk</strong></td>
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<tr>
<td><strong>Low-frequency 3dB cut-off</strong></td>
<td>0.02-500 Hz</td>
<td><strong>Amplifier input capacitance</strong></td>
</tr>
<tr>
<td><strong>High-frequency 3dB cut-off</strong></td>
<td>100-20 kHz</td>
<td><strong>Amplifier reference Input capacitance</strong></td>
</tr>
<tr>
<td><strong>Amplifier AC input range</strong></td>
<td>±6.4 mV</td>
<td><strong>Amplifier Input Impedance</strong></td>
</tr>
<tr>
<td><strong>Amplifier DC input range</strong></td>
<td>± 0.4 mV</td>
<td><strong>Amplifier reference Input impedance</strong></td>
</tr>
<tr>
<td><strong>Amplifier input-referred offset voltage</strong></td>
<td>&lt; ±100 μV</td>
<td><strong>Amplifier input-referred noise</strong></td>
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SOFTWARE ENVIRONMENT

- GUI for device configuration and real-time data display
- Individual channel is displayed as a subpanel for flexible viewing arrangements
- MATLAB Based GUI for offline clustering
- Template and configurations are generated with WaveClus
- Display of template matching output
- Each event is represented as a vertical bar
**Experimental Process Flow**

On startup an initial configuration is loaded from a PC based configuration GUI. The raw neural signal is then digitised by the analogue front-end (currently Intan RHD2132) and passes directly through the FPGA to the computer to be stored.

A Matlab GUI is provided for offline clustering. The underlying method is based on WaveClus. The GUI allows the user to visualize different templates and associated spikes together with accuracy and false alarm rate estimation. The user can automatically generate templates for all 32 channels or manually do it on selected channels. The following parameters will be uploaded after template generation:

- Spike detection thresholds (per channel)
- Spike templates (4 per channel), 16x 9-bit samples per template.
- Template matching thresholds (per channel)

The configuration will be saved in a binary file and uploaded by the configuration GUI to the FPGA. Alternative clustering methods or software can be used to generate the required templates/configuration data.

**Learning Phase** — Raw signal output

**Autonomous Phase** — Spike sorting output

Once the FPGA has valid templates & thresholds it can be put into template matching mode. In this mode the FPGA evaluates all the incoming data against assigned templates using sum of absolute distance method. The best matching template with a score below the programmed threshold would signal a matching event to the computer. This matching event would report the matching time, channel number and template ID.
**TEMPLATE-BASED SPIKE SORTING**

Similarity Quantifier

*Distance based* template matching method. Colour traces are templates. Black traces are input signals. The score is the sum of distances between signals and templates. The matching template achieves the lowest score that is below a user set threshold.

**DEVELOPMENT ROADMAP**

Upcoming Features (in development):

- Standalone recording solution with wireless access
- LFP and spike recording over the same area
- Thousands of channels recording and sorting
- Single-chip Application Specific Integrated Circuit (ASIC) solution

<table>
<thead>
<tr>
<th>Version</th>
<th>Features</th>
<th>Power (mW)</th>
<th>Dimensions and Weight</th>
<th>Ch. per module (max. # of mod.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NGNI-V1 (Q2 2016)</td>
<td>AP, SS, SPI, USB3</td>
<td>34</td>
<td>26mm x 14mm x 4mm, ~2g</td>
<td>32/64/96 (x1)</td>
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<tr>
<td><strong>Evaluation system available soon</strong></td>
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<tr>
<td>NGNI-V2 (Q4 2016)</td>
<td>AP, LFP, SS, SPI, USB3</td>
<td>~15</td>
<td>26mm x 14mm x 6mm, ~3g</td>
<td>64/128/192 (x8)</td>
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AP = “raw” extracellular action potential recording, LFP = “raw” local field potential recording, SS = Realtime spike sorting, SPI= Local, auxiliary SPI output, USB3= Host interface using USB3 bridge
PRELIMINARY IN-VIVO RECORDING AND SPIKE SORTING RESULTS

Experimental measurements taken on NHP with tungsten microwire electrodes implanted in Motor and Premotor Cortex. Front-end configured for a signal band of 300Hz-3kHz with digital high pass filter set at 318Hz.

Data plotted using Matlab shown below.

Different unit events (classified spikes) indicated by coloured crosses. Associated templates shown in sub-plots above.

Noise level recorded at 12.7 μV (limited by experimental measurement, not platform).

References


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