IMPERIAL

Module Specification

Basic details

UID		Cohorts covered (Earliest cohort)	
Long title	Digital Electronics and Computer Architecture		
New code	ELEC40003	New short title	
Brief description of module *(approx. 600 chars.)*	The aim of this module is to teach the foundations of digital design and low-level computer operation and enable you to understand system design across the hardware -software boundary		
Available as a standalone module/ short course?	N		

Statutory details

	ECTS	CATS	Non-credit	
Credit value	10	20	N	HECOS codes
FHEQ level	Level 4			

Allocation of study hours

	Hours	
Lectures	38	
Group teaching	19	*Incl. seminars, tutorials, problem classes.*
Lab/ practical	44	
Other scheduled		*Incl. project supervision, fieldwork, external visits.*
Independent study	149	*Incl. wider reading/ practice, follow-up work, completion of assess*
Placement		*Incl. work-based learning and study that occurs overseas.*
Total hours	250	
ECTS ratio	25.00	

Project/placement activity

Is placement activity allowed?	No

Module delivery

Delivery mode	Taught/ Campus	Other	
Delivery term		Other	Term 1; Term 2

Ownership

Primary department	Electical and Electronic Engineering
Additional teaching departments	
Delivery campus	South Kensington

Collaborative delivery

Collaborative delivery?	N

External institution	N/A
External department	N/A
External campus	N/A

Associated staff

Role	CID	Given name	Surname
Module Leader		Tom	Clarke
Topic Leader		George	Constantinides

Learning and teaching

Module description

Learning outcomes	Upon successful completion of this module, you will be able to: 1. design significant synchronous sequential digital circuits using registers and combinational logic 2. design simple two's complement addition and subtraction digital circuits, with correct use of carry and overflow. 3. use digital blocks: RAMs, ROMs, registers, adders, multiplexers and state machines to design and analyse the operation of simple pipelined RISC computer systems. 4. model the operation of machine code instructions on a CPU at register-transfer level, and manipulate data using different numeric representations. 5. write programs for arithmetic operations, manipulating bit fields within words, accessing memory, and calling subroutines. 6. implement I/O in embedded computer systems using polling.
Module content	First an introduction will be provided to the design and operation of digital electronic circuits. The course will cover: (1) Data representation for digital electronics (2) Boolean Algebra and Combination Logic. (3) Combinational logic gates, circuit and logical operation, and their implementation. (4) Basic digital blocks e.g. multiplexers, adders, encoders/decoders, flip-flops, ROM/RAM, registers. (5) Sequential Circuits and their timing, State Machines. (6) Simple application examples to tie together the above concepts. Then you will apply this knowledge to the design of a simple CPU. The module will culminate with the design of hardware and code for an embedded processor. Key laboratory skills instruction on how to use equipment and analyse measured data.
Learning and Teaching Approach	The lectures will be taught in a large lecture theatre to the whole year group using powerpoint slides. These lectures will be recorded for revision purposes and released at the end of each week. Problem solving classes with ½ of the cohort will be based on team based learning principles. You will form teams of 6 students. Team will work in-class for peer instruction. The module lecturer will answer questions and go through more complex problems. In tutorial groups of 3-4 students you will have the opportunity to solve a selection of problems with your personal tutor. Laboratory exercises will link the topics taught directly to their applications. Simulations using Quartus will be part of the learning in applied settings.

Assessment Strategy	Formative assessment: In-class team work will give you opportunity to practice your learned skills. The solutions to the problems will be discussed but will not be marked. For the lab, there will be mid term interviews with GTAs. Summative assessment: These assessments happen under time constraint and in an exam environment. The marks on these assessments will count towards your final degree. There will be 3 assessment types and 5 assessment events: Mid Autumn term computer based confidence test (theory and problems) – 5% End Autumn term lab orals and demonstrations – 15% Mid Spring term computer based competence test (theory and problems) – 5% End Spring term lab orals and demonstrations – 15% Start of Summer term exam – 60%
Feedback	The correct answers on the on-line test will be distributed after the tests are completed. Poorly understood topics will be discussed during the TBL classes. Feedback on the oral laboratory exam will be given after the assessments. Feedback on the exams will be given after the Supplementary Qualifying Tests have ended and the September examiners meeting passed. This feedback will come in the form of annotated example answers. The annotations will highlight where the student cohort did well and where general problems in understanding were observed.
Reading list	1. "Digital Systems – Principles and Applications", 10th Ed, R. J. Tocci, N. S. Widmer, G. Moss, Pearson, 2007 2. "Digital Fundamentals with PLD Programming", 10th Ed, T.L. Floyd, Prentice Hall, June 2008 3. "Digital design : principles and practices", J. F. Wakerly, Upper Saddle River, NJ : Pearson/Prentice Hall 2006 4th Ed. 4. Computer Organization and Design, Revised Printing, Third Edition: The Hardware/Software Interface. Patterson and Hennessy 2004 5. ARM Assembly language. J.R. Gibson
Required equipment/ software	NA

Quality assurance

Date of first approval	October 2019
Date of last revision	January 2025
Date of this approval	
Module leader	Tom Clarke

Office use only

QA Lead	
Department staff	
Date of collection	
Date exported	
Date imported	

Notes/ comments

Template version

Assessment details

Grading method	Numeric	Pass mark	40%

Assessments

Assessment type	Assessment description	Weighting	Pass mark	Must pass?
Practical	Autumn end of term laboratory practicals (orals and demonstration)	15%	40%	N
Examination	Autumn midterm computer based test	5%	40%	N
Practical	Spring end of term laboratory practicals (orals and demonstration)	15%	40%	N
Examination	Spring midterm computer based test	5%	40%	N
Examination	Exam at start of summer term	60%	40%	N
		100%		