IMPERIAL

Module Specification

Basic details

UID		Cohorts covered (Earliest cohort)	
Long title	Circuits and Systems		
New code	ELEC50001	New short title	
Brief description of module *(approx. 600 chars.)*	This module builds on the first-year modules relating to analogue and digital circuits, computer architecture, and programming, to teach students how to analyse and design electronic circuits with a system level perspective. The aim of this module is to provide students with the theoretical foundations, the design techniques and hands-on experiences of acquiring physical analogue signals, pre-processing them, converting into digital form, then process these in a digital programmable hardware on both a microprocessor and on a Field Programmable Gate Array (FPGA). Unlike Year 1 module on circuits, this year students will learn to process signals that have noise and electronic hardware that are non-ideal.		
Available as a standalone module/ short course?	N		

Statutory details

	ECTS	CATS	Non-credit	
Credit value	7.5	15	N	HECOS codes
FHEQ level	Level 5			

Allocation of study hours

	Hours	
Lectures	15	
Group teaching	7	*Incl. seminars, tutorials, problem classes.*
Lab/ practical	32	
Other scheduled		*Incl. project supervision, fieldwork, external visits.*
Independent study	133.5	*Incl. wider reading/ practice, follow-up work, completion of assess*
Placement		*Incl. work-based learning and study that occurs overseas.*
Total hours	187.5	
ECTS ratio	25.00	

Project/placement activity

Is placement activity allowed?	No

Module delivery

Delivery mode	Taught/ Campus	Other	
Delivery term	Term 1	Other	

Ownership

Primary department	Electical and Electronic Engineering
Additional teaching	

departments	
Delivery campus	South Kensington

Collaborative delivery

Collaborative delivery?	N
External institution	N/A
External department	N/A
External campus	N/A

Associated staff

Role	CID	Given name	Surname
Module Leader		Peter	Cheung

Learning and teaching

Module description

Learning outcomes	On successful completion of this module, students should be able to: • Design, analyse and explain sensors analogue circuit interfaces between the input and digital signal processing phase. • Explain the common type of DAC and ADC architectures currently used in industry • Design low-pass, high-pass and band-pass filters for preconditioning signals • Choose suitable low-noise pre-amplifiers and analyse its impact on noise performance of the system • Choose suitable output circuit architecture for high current drive and design a circuit to meet specification • Design reasonably complex circuits involving digital building blocks such as shift register, RAM and FSM, and interface them to a processor • Write good quality Verilog code to specify digital hardware • Implement digital hardware on an FPGA • Design a basic testbench circuit
Module content	Topics to be covered are: • Sensors • Sampling and quantization of signals • Data conversion and converters • Analogue filters • High current drive circuits • Digital building blocks (e.g. shift registers, RAM/ROM, Multipliers) • FPGA architectures • Finite State Machine (FSM) Design • Digital interfacing • Digital Design in Verilog HDL • Testbench designs

Learning and Teaching Approach	The lectures will be time tabled multi mode teaching that takes place in the class room with max 30 students who have obtained a booked place. These lectures will be streamed on MS Teams and be recorded. The recordings will be made accessible on Panopto. Recordings are for students living in other time zones, all other students are strongly advised to be present during the life streaming. All problem classes will be carried out remote synchronous and will be time tabled. Problem classes consist of 100 students/Teams with different break out channels for different student groups. The module lecturer and GTAs will support these sessions. The problem classes will focus on applying the techniques covered in lectures to a variety of problems ranging from the easy to the difficult, with the chance to ask questions and get one-to-one help. These classes will involve both individual as well as group work. Labs are an integral part of this module and are time tabled multi mode sessions in the level 1 labs. A max of 60 students can be allowed in the lab. Students will need to book their lab space. The lab is built on the lab-in-a-box concept and all students whether remote or in class will be required to work with this lab equipment.
Assessment Strategy	There will be computer-based test in the midterm week. The laboratory work is a part of the module assessment. This assessment will be based on an oral exam that evaluates your understanding of the concepts and your ability to explain and build the experimental set-up. The final exam will cover all the topics in the module.
Feedback	Feedback will be given in the exercise classes. The on-line tests will generate automatic feedback. Feedback on the oral laboratory exam will be given after the assessments. Feedback on the exams will be given after the Supplementary Qualifying Tests (Sept). This feedback will come in the form of annotated example answers. The annotations will highlight where the student cohort did well and where general problems in understanding were observed.
Reading list	
Required equipment/ software	NA

Quality assurance

Date of first approval	
Date of last revision	
Date of this approval	July 2025
Module leader	Peter Cheung
Notes/ comments	

Office use only

QA Lead	
Department staff	
Date of collection	
Date exported	
Date imported	

Template version

Assessment details

Grading method	Numeric	Pass mark	40%

Assessments

Assessment type	Assessment description	Weighting	Pass mark	Must pass?
Laboratory	Autumn mid-term lab oral	15%	40%	N
Laboratory	Autumn end of term lab oral	25%	40%	N
Examination	exam at start of summer term	60%	40%	N
		100%		