IMPERIAL

Module Specification

Basic details

UID		Cohorts covered (Earliest cohort)	
Long title	Information Processing		
New code	ELEC50009	New short title	

Brief description of module *(approx. 600 chars.)*

The aim of the module is to enable students to design information processing systems of medium complexity, by considering communication and computation costs, as well as local (embedded) and server-side processing. The module builds upon the material you have been taught in your EIE year two, and introduces the practical aspects of embedded processing, networking, and databases. The first part of the module consists of a series of practical labs where you will be exposed to the practical aspects of embedded processing, networking and datasets, followed by a practical component (i.e. coursework) with strong emphasis on the design methodology, where a fully operational processing system needs to be designed

Available as a standalone module/ short course? N

Statutory details

	ECTS	CATS	Non-credit	
Credit value	5	10	N	HECOS codes
FHEQ level	Level 5			

Allocation of study hours

	Hours	
Lectures	5	*5 lectures in the first part of the term*
Group teaching	0	
Lab/ practical	10	*5 2-hour labs in the first part of the term*
Other scheduled	8	*4 2-hour sessions in the second part of the term with GTA support*
Independent study	102	*95 hours independent study*
Placement		
Total hours	125	
ECTS ratio	25.00	

Project/placement activity

Is placement activity allowed? No

Module delivery

Delivery mode	Taught/ Campus	Other	
Delivery term	Term 2	Other	

Ownership

Primary department	Electrical and Electronic Engineering
Additional teaching departments	

Delivery campus	South Kensington

Collaborative delivery

Collaborative delivery?	N
External institution	N/A
External department	N/A
External campus	N/A

Associated staff

Role	CID	Given name	Surname
Module Leader		Ed	Stott
Topic Leader		Mirza Muhammad Sarim	Baig

Learning and teaching

Module description

Learning outcomes	Upon successful completion of this module, you will be able to: 1. Develop an embedded system based on a CPU/FPGA 2. Apply signal processing, techniques to a time-series data considering their computational cost 3. Develop the communication infrastructure between a local node and a server 4. Describe a relational database design and use relational operators 5. Use relational databases to answer complex data queries in SQL 6. Design a database that communicates with the rest of the system 7. Judge the compute capabilities of different platform
Module content	In this module the principles and techniques for designing information processing system will be studied. The module covers the following topics: - Introduction to Field Programmable Gate Arrays (FPGA) - Introduction to the design process of a digital system using an FPGA - Soft core CPU (NIOSII) architecture - Interfacing a CPU with external peripherals - UART and SPI interfaces - Designing a relational database and applying SQL - Establishing a communication with a AWS server - Instantiate a database on a remote server
Learning and Teaching Approach	The teaching of the module consists of two parts. In the first part (starting of the term till the midterm week), there will be lectures and a series of labs. During the lectures, you will be introduced to a number of new concepts around the practical aspects of information processing, as well as a short introduction to the followed up lab will be provided. Each lecture is followed by a lab where you will put in practice the concepts that you saw during the lecture in a structured way. In the second part, (after the midterms week till the end of the term), you will focus on your project, and time-tabled slots will be scheduled where GTA help will be provided.

Assessment Strategy	Working in a group of 5-6 people, you will be asked to design an information processing systems that has certain elements (local and server-side processing, communication over a network and use of a database). During the midterm week, you will be examined on your understanding of the design process of such system, based on the designed labs, and you will be provided with formative feedback. The summative assessment of the module will be done in the last week of the term, where you will have to demonstrate your system, answer technical questions (oral examination), and provide a report on your work. The module has also a peer assessment element.
Feedback	You will be provided with oral feedback during the labs (first part of the module), as well as on your planned system. Written comments will be provided on your report submission.
Reading list	The reading list will be provided in session
Required equipment/ software	NA

Quality assurance

Date of first approval	
Date of last revision	July 2026
Date of this approval	July 2026
Module leader	Ed Stott
Notes/ comments	updated 9 Sept 2026

Office use only

QA Lead	
Department staff	
Date of collection	
Date exported	
Date imported	

Template version

Assessment details

Grading method	Numeric	Pass mark	40%

Assessments

Assessment type	Assessment description	Weighting	Pass mark	Must pass?
Coursework	Working system presentation, Report	80%	40%	N
Practical	Mid term lab oral	20%	40%	N
		100%		