IMPERIAL

Module Specification

Basic details

UID		Cohorts covered (Earliest cohort)	
Long title	Digital Systems Design		
New code	ELEC60011	New short title	
Brief description of module *(approx. 600 chars.)*	The aim of the module is to enable students to be able to design digital systems of medium complexity, by covering topics on system architecture, pocessors, communication and memory. The module is complemented by a practical component (i.e. coursework) with strong emphasis on the design methodolody in the case where an FPGA device is targeted, where a fully operational processing system needs to be designed, enabling students to apply in practice the theory that have been taught and to consider performance-resource trade-offs.		
Available as a standalone module/ short course?	No		

Statutory details

	ECTS	CATS	Non-credit	
Credit value	5	10	N	HECOS codes
FHEQ level	6			

Allocation of study hours

	Hours	
Lectures	20	
Group teaching	0	*Incl. seminars, tutorials, problem classes.*
Lab/ practical	0	
Other scheduled	10	*Incl. project supervision, fieldwork, external visits.*
Independent study	95	*Incl. wider reading/ practice, follow-up work, completion of assess*
Placement	0	*Incl. work-based learning and study that occurs overseas.*
Total hours	125	
ECTS ratio	25.00	

Project/placement activity

Is placement activity allowed?	0

Module delivery

Delivery mode	Taught/ Campus	Other	
Delivery term	Term 2	Other	

Ownership

Primary department	Department of Electrical and Electronic Engineering
Additional teaching departments	

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Delivery campus	South Kensington

Collaborative delivery

Collaborative delivery?	0
External institution	
External department	
External campus	

Associated staff

Role	CID	Given name	Surname
Module leader		Christos-Savvas	Bouganis

Learning and teaching

Module description

Learning outcomes	Upon successful completion of this module, you will be able to: 1. design complex, high performance digital systems 2. use a modern CAD tool to help with the design 3. implement such designs using programmable logic (e.g. FPGAs) 4. design with digital building blocks (such as memory chips, microprocessors, arithmetic circuits etc.)
Module content	In this module the principles and techniques for designing reasonably large digital circuits and systems will be studied. Based on the design of a practical medium-sized circuit, and a number of smaller examples, the module covers the following topics: System bus interfacing; FPGA architectures; Multiplier circuits; Dynamic memory interfacing and DMA control circuits; Timing issues in digital circuits: hazards, metastability and races; High-speed digital design techniques;
Learning and Teaching Approach	There will be recordings to support the delivery of the material, combined with additional in-person classes where case studies will be discussed, as well as to provide a forum for questions on the recording material to be raised. You will be provided with introductory exercises and tutorials to familiarise yourself with the FPGA platform board; and additional reading material on FPGA architectures.

Assessment Strategy	Coursework (85%). You will design an embedded system using a FPGA. You will use a vendor's specific software which you can download for use at home, or is installed on the Department's computers. You will be allocated an FPGA board on which to build your project. The objective of the coursework is to accelerate an application through reconfigurable hardware. You have to produce three reports and a working demonstrator. Whole group feedback will be provided during lectures on the three deliverables. Test (15%). You will be assessed on your understanding of the material through an on-online test (such as wiseflow).
Feedback	You will be provided with written comments on coursework submissions.
Reading list	There are no prefect textbooks for this module. Herte are five reasonable possibilities: 1) Wakerly, J.F: Digital Design Principles and Practices, Prentice Hall, 4th ed, 2005. 2) Koren, I: Computer Arithmetic Algorithms, A.K. Peters Ltd, 2nd ed. 3) Boriello, G., & Katz, R.: Contemporary Logic Design, Prentice Hall, 2004. 4) Johnson, H.G.: High-Speed Digital System Design: a handbook of black magic, Prentice Hall, 1993. 5) Wolf, W.: FPGA-based System Design, Prentice Hall, 2004.

Quality assurance

Date of first approval	August 2021
Date of last revision	May-24
Date of this approval	May 2025
Module leader	Dr Christos-Savvas Bouganis
Notes/ comments	

Office use only

QA Lead	
Department staff	
Date of collection	
Date exported	
Date imported	

Template version

Assessment details

Grading method	Numerical	Pass mark	40%

Assessments

Assessment type	Assessment description	Weighting	Pass mark	Must pass?
Coursework	Design a basic system	0%		N
Coursework	Extend the basic system with extra functionality (i.e. embedded mulitpliers and off-chip memory) and compute a more complex function	25%	40%	N
Coursework	Extend the previous system with custom IP blocks for minimising the latency of function evaluation (design a CORDIC IP block and consider various architectures)	45%	40%	N
Practical	Presentation and interview	15%	40%	N
Examination	Wiseflow test	15%	40%	N
		100%		