IMPERIAL

Module Specification

Basic details

UID		Cohorts covered	Earliest cohort: Latest c:
Long title	Full-Custom Integrated Circuit Design		
New code	ELEC70012	New short title	

Brief description of module *(approx. 600 chars.)*

CMOS Technology is currently the industry mainstream for the vast majority of all analogue, digital and mixed-signal integrated circuits. Most modern day consumer electronics including microprocessors, mobile phones, digital cameras are all implemented using CMOS technology. The module will focus on the CMOS integrated circuit technology covering the basic fundamentals as well as more advanced topics, and go through the design process for full custom chip design used for both analogue and digital microelectronics.

519 characters

Available as a standalone module/ short course? No

Statutory details

	ECTS	CATS	Non-credit	HECOS codes
Credit value	5	10	N	
FHEQ level	L7			

Allocation of study hours

	Hours	
Lectures	20	
Group teaching	0	*Incl. seminars, tutorials, problem classes.*
Lab/ practical	25	
Other scheduled	0	*Incl. project supervision, fieldwork, external visits.*
Independent study	80	*Incl. wider reading/ practice, follow-up work, completion of assessments*
Placement	0	*Incl. work-based learning and study that occurs overseas.*
Total hours	125	
ECTS ratio	25.00	

Project/placement activity

Is placement activity allowed? No

Module delivery

Delivery mode	Taught/ Campus	Other	
Delivery term	Term 2	Other	

Ownership

Primary department	Department of Electrical and Electronic Engineering
Additional teaching departments	0

Delivery campus	South Kensington

Collaborative delivery

Collaborative delivery?	0
External institution	
External department	
External campus	

Associated staff

Role	CID	Given name	Surname
Module Leader		Tim	Constandinou
		0	0
		0	0
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		0	0
		0	0

Learning and teaching

Module description

Learning outcomes	Upon successful completion of this module, you will be able to: 1. Explain key features, limitations and topics related to CMOS technology 2. Describe full custom integrated circuit design methodology and issues/constraints related to analogue/digital/mixed signal circuit design. 3. Design and assess full custom integrated circuit layouts 4. Use a complete tool suite (schematic capture, simulation, layout design, physical verification) covering the full custom design of CMOS integrated circuits.
Module content	Microelectronics; Digital circuits; Circuit simulation; CMOS fabrication; CMOS devices; Layout design; Layout verification; Analogue design; Data converters; Advanced topics in full-custom IC design
Learning and Teaching Approach	The module is delivered through a combination of lectures, laboratories and project. The module starts with 5 weeks of lectures covering CMOS technology, analogue and digital circuit design, and EDA tools. Alongside these lectures are four assessed laboratories that introduce you to Cadence. From week 5 you will work on full custom IC design project supported through GTA-attended lab workshops and online forum for Q&A.
Assessment Strategy	This module is assessed through coursework (100%). Through the laboratory and project you will learn CAD tools for full custom IC design using Cadence. The three labs cover: (1) inverter and ring oscillator design and simulation; (2) ring oscillator layout, post-layout and process variation simulation; (3) amplifier design and layout. The labs are assessed by logbook (week 5) which contributes 30% to the module mark. The lecture content is assessed through an oral test (week 8) which contributes 30% to the module mark. The individual project is assessed through a final report (week 11) which contributes 40% to the module mark.
Feedback	Summative feedback will be provided through written comments for each of the 3 deliverables (lab logbook and final report) as well as feedback will be provided for the oral test. Formative feedback will be available to you through discussion with the module leader and GTAs
Reading list	CORE 1) Baker, R.J.: CMOS: circuit design, layout and simulation, IEEE Press/John Wiley & SOns, 3rd, 2010. SUPPLEMENTARY 1) West, N.H.E., & Harris, D.M.: Integrated Circuit Design, Pearson Prentice Hall, 4th ed, 2011. 2) Hastings, A.: Art of Analog Layout, the, Pearson Prentice Hall, 2nd, 2006

Quality assurance

Date of first approval	July 2023
Date of last revision	February 2026
Date of this approval	
Module leader	Prof Tim Constandinou
Notes/ comments	

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QA Lead	
Department staff	
Date of collection	
Date exported	
Date imported	

Template version #####

Assessment details

Grading method	Numerical	Pass mark	50%

Assessments

Assessment type	Assessment description	Weighting	Pass mark	Must pass?
Coursework	Logbook for labs 1-3	30%	50%	N
Coursework	Oral test	30%	50%	N
Coursework	Final report	40%	50%	N
0	0	0%	0%	0.00
0	0	0%	0%	0.00
0	0	0%	0%	0.00
0	0	0%	0%	0.00
0	0	0%	0%	0.00
0	0	0%	0%	0.00
0	0	0%	0%	0.00
0	0	0%	0%	0.00
0	0	0%	0%	0.00
0	0	0%	0%	0.00
0	0	0%	0%	0.00
0	0	0%	0%	0.00
		100%		