IMPERIAL

Module Specification

Basic details

UID		Cohorts covered	Earliest cohort: Latest c:
Long title	Advanced Digital Systems Design		
New code	ELEC70046	New short title	
Brief description of module *(approx. 600 chars.)*	The aim of the module is to enable you to design digital systems of medium complexity, by covering topics on system architecture, pocessors, communication and memory. The module is complemented by a practical component (i.e. coursework) with strong emphasis on the design methodolody in the case where an FPGA device is targeted, where a fully operational processing system needs to be designed, enabling you to apply in practice the theory that have been taught and to consider performance-resource trade-offs. The module also exposes you to modern tools for hardware design, by focusing on High Level Synthesis (HLS) hardware description.		

641 characters

Available as a standalone module/ short course? No

Statutory details

	ECTS	CATS	Non-credit	
Credit value	5	10	N	HECOS codes
FHEQ level	7			

Allocation of study hours

	Hours	
Lectures	20	
Group teaching	0	*Incl. seminars, tutorials, problem classes.*
Lab/ practical	0	
Other scheduled	10	*Incl. project supervision, fieldwork, external visits.*
Independent study	95	*Incl. wider reading/ practice, follow-up work, completion of assessments*
Placement	0	*Incl. work-based learning and study that occurs overseas.*
Total hours	125	
ECTS ratio	25.00	

Project/placement activity

Is placement activity allowed? No

Module delivery

Delivery mode	Taught/ Campus	Other	
Delivery term	Term 2	Other	

Ownership

Primary department	Department of Electrical and Electronic Engineering
Additional teaching departments	

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Delivery campus	South Kensington

Collaborative delivery

Collaborative delivery?	No
External institution	
External department	
External campus	

Associated staff

Role	CID	Given name	Surname
Module leader		Christos	Savvas-Bouganis

Learning and teaching

Module description

Learning outcomes	On successful completion of the module, you should be able to: a) Design a Digital System using modern CAD tools and HLS language b) Analyse the performance of a digital system c) Optimise a digital system for performance (latency, throughput) d) Propose an architecture that meets resource and performance specifications
Module content	In this module the principles and techniques for designing reasonably large digital circuits and systems will be studied. Based on the design of a practical medium-sized circuit, and a number of smaller examples, the module covers the following topics: System bus interfacing; FPGA architectures; Multiplier circuits; Dynamic memory interfacing and DMA control circuits; Timing issues in digital circuits: hazards, metastability and races; High-speed digital design techniques;
Learning and Teaching Approach	The teching is based on a mix of a flipped classroom approach and in-person teching for material delivery and problem discussion. Additional classes (study groups) can also be arranged on an ad-hoc basis if there is enough demand for them. You will be provided with introductory exercises and tutorials to familiarise yourself with the FPGA development board; and additional reading material on FPGA architectures.

Assessment Strategy	This module is assessed via Coursework (85%). Working in pairs, you will design an embedded system using an FPGA. The objective of the coursework is to accelerate an application through reconfigurable hardware, by deriving an optimised hardware architecture. You have to produce two reports and a working demonstrator. The first report is of low-stakes and it is used mainly for formative evaluation (i.e. monitor your progress and provide early feedback on your work), where the second report and the demonstrator are used for summatve evaluation. Whole group feedback on the two deliverables will be provided during the scheduled lectures. Test (15%). You will be assessed on your understanding of the material through an on-line test (such as wiseflow).
Feedback	You will be provided with written comments on coursework submissions, as well as best practices for both formative and summative evaluation parts will be discussed in the lectures.
Reading list	There are no prefect textbooks for this module. Herte are five reasonable possibilities: 1) Wakerly, J.F: Digital Design Principles and Practices, Prentice Hall, 4th ed, 2005. 2) Koren, I: Computer Arithmetic Algorithms, A.K. Peters Ltd, 2nd ed. 3) Boriello, G., & Katz, R.: Contemporary Logic Design, Prentice Hall, 2004. 4) Johnson, H.G.: High-Speed Digital System Design: a handbook of black magic, Prentice Hall, 1993. 5) Wolf, W.: FPGA-based System Design, Prentice Hall, 2004.

Quality assurance

Date of first approval	
Date of last revision	July 2026
Date of this approval	
Module leader	Christos-Savvas Bouganis

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QA Lead	
Department staff	
Date of collection	
Date exported	
Date imported	

Notes/ comments	

Template version #####

Assessment details

Grading method	Numerical	Pass mark	50%

Assessments

Assessment type	Assessment description	Weighting	Pass mark	Must pass?
Coursework	Design a basic embedded system on an FPGA and demonstrate its working with a simple function evaluation.	15%	50%	N
Coursework	Build a system for the acceleration of an ML algorithm using a processor and the FPGA fabric.	55%	50%	N
Practical	Presentation and interview	15%	50%	N
Examination	Test	15%	50%	N
		100%		