IMPERIAL

Module Specification

Basic details

UID		Cohorts covered (Earliest cohort)	
Long title	Laboratory in ADIC		
New code	ELEC70093	New short title	
Brief description of module *(approx. 600 chars.)*	This lab aims to develop advanced skills in utilising industry-strength Electronic Design Automation (EDA) tools for microelectronic design. The lab comprises of three topics: Digital Design, Digital System Design, IC Design. Tools and design flows include the Cadence Design Systems (CDS) for full-custom analogue/mixed signal, and standard-cell digital, digital Systems on Chip (SoC) design using the latest toolflows from Xilinx, an FPGA vendor for practical skills in designing digital systems that include hardcore processors interfaced with FPGA logic.		
Available as a standalone module/ short course?	N		

Statutory details

	ECTS	CATS	Non-credit	
Credit value	10	20	N	HECOS codes
FHEQ level	Level 7			

Allocation of study hours

	Hours	
Lectures	8	
Group teaching		*Incl. seminars, tutorials, problem classes.*
Lab/ practical	34	*Inc. professional and research skills training*
Other scheduled		*Incl. project supervision, fieldwork, external visits.*
Independent study	208	*Incl. wider reading/ practice, follow-up work, completion of assess*
Placement		*Incl. work-based learning and study that occurs overseas.*
Total hours	250	
ECTS ratio	25.00	

Project/placement activity

Is placement activity allowed?	No

Module delivery

Delivery mode	Taught/ Campus	Other	
Delivery term		Other	Term 1 and Term 2

Ownership

Primary department	Electrical and Electronic Engineering
Additional teaching departments	

Delivery campus	South Kensington

Collaborative delivery

Collaborative delivery?	N
External institution	
External department	
External campus	

Associated staff

Role	CID	Given name	Surname
Module Leader		Christos	Papavassiliou
Lecturer		Sam	Coward
Lecturer		Tim	Constandinou

Learning and teaching

Module description

Learning outcomes	After completion of this lab, you will be able to: 1) Evaluate the issues associated with modern IC manufacture processes and the various testing methodologies. 2) Evaluate the full custom design flow for analogue and digital integrated circuits in CDS. 3) Recognise the essential features of programmable logic devices (FPGAs) and how they are built. 4) Use Verilog to design combinational and sequential circuits, applying the principles of digital hardware design on FPGAs. 5) Evaluate and analyse the issues associated with modern SoC systems and develop digital Systems-on-Chip using FPGAs through Xilinx's toolflow. 6) Consider and justify communication protocols between the processor and an integrated IP and evaluate and model the design flow for integrating a VHDL and HLS based IP with the processor
Module content	Cadence: 1) Introduction to AMS 0.35um process 2) Simulation of PSRR, CMRR; Stability analysis 3) Noise analysis; Monte-Carlo analysis; Corner analysis 4) Periodic Steady State (PSS) analysis; Periodic AC (PAC) analysis 5) General guidelines for analogue layout; Perform post-extraction simulations Digital Design Lab: 1) Introduction to integrated circuits and programmable logic devices (FPGAs). 2) Schematic hardware design versus textual hardware description languages. 3) Introduction to the Verilog language. 4) Moore and Mealy machines. 5) Designing finite state machines in Verilog. 6) Analogue-to-digital conversion and digital-to-analogue conversion. 7) Serial-to-parallel and parallel-to-serial interfaces. 8) Design of a voice echo synthesiser. DSD: 1) Synthesis digital circuitry with Cadence RC and Encounter 1) Introduction to the Zynq platform 2) Design of a SoC system to control the LEDs on the board (HW and SW)
Pattern of learning	

Learning and Teaching Approach	The teaching is based on lab activities, where an introductory lecture will be provided at the start of each lab, as well as a discussion will follow towards the end of the lab to clarify the lab's topics.The work is carried out in groups (for more than 50% of the activities).
Assessment Strategy	The lab components are assessed through a blackboard test, oral examinations and submitted reports, that aim to assess your understanding of the topics seen during the labs. These will be assessed accordingly: Cadence - Blackboard Test. Digital Design - Oral Examination. DSD - Oral Examination. Regarding the arrangements for returning marked work, students can expect to receive their provisional letter grades first. These provisional marks will give students an early indication of their performance before the final grades are officially released. Feedback on student performance in the summative assessments will be provided after the final grades have been confirmed. This feedback will be comprehensive and include comments on your strengths and areas for improvement, as observed in each component of the lab assessment. A self-reflection on the performance of the team and of the individual as part of the team will also be assessed in in a written report. You will need to desribe team organisation, your role within the team, effectiveness of own contribution and reflection on team working skills acquired.
Feedback	Students would recieve formative feedback by the lab leaders and teaching assistants during the lab sessions based on their progress and resutls. Students will be provided with oral feedback on your progress during the lab exercise, where summative feedback will be provided after the oral examination. Students will receive summative feedback immediately after completing the blackboard test. Finally, students will receive summative feedback two working weeks after submitting the report.
Reading list	Cadence: CMOS Circuit Design, Layout, and Simulation - R. Jacob Baker, DSD: The Zynq Book Tutorials for Zybo and ZedBoard, The Zynq Book ,Vivado Design Suite User Guide: Hiigh-Level Synthesis

Quality assurance

Date of first approval	February 2022	
Date of last revision	June 2026	Is
Date of this approval		
Module leader	Christos Papavassiliou	

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QA Lead	
Department staff	
Date of collection	
Date exported	
Date imported	

Notes/ comments

Template version

Assessment details

Grading method	Pass/Fail	Pass mark	100%

Assessments

Assessment type	Assessment description	Weighting	Pass mark	Must pass?
Examination	Blackboard Test on Cadence	33%	50%	N
Practical	Oral examination on digital design	33%	50%	N
Practical	Oral examination on DSD	34%	50%	N
Coursework	Self-reflection on individual performance as part of the team	0%	100%	Y
		100%	63%	Y