IMPERIAL

Module Specification

Basic details

UID		Cohorts covered (Earliest cohort)	
Long title	Digital VLSI System-on-Chip (SoC) Design		
New code	ELEC70142	New short title	
Brief description of module *(approx. 600 chars.)*	This elective module provides knowledge and skills required to design a complex digital VLSI design from conception to fabrication. Students will learn to use industrial grade CAD environment and tools to design digital system-on-chip circuits using full-custom editing tools and HDL to gate synthesis tools. They will learn the entire design and verification tool flow and produce a moderately complex digital chip suitable for fabrication at a silicon foundry (e.g. TSMC)		
Available as a standalone module/ short course?	N		

Statutory details

	ECTS	CATS	Non-credit	
Credit value	5	10	N	HECOS codes
FHEQ level	Level 7			

Allocation of study hours

	Hours	
Lectures	20	
Group teaching		*Incl. seminars, tutorials, problem classes.*
Lab/ practical	30	
Other scheduled		*Incl. project supervision, fieldwork, external visits.*
Independent study	75	*Incl. wider reading/ practice, follow-up work, completion of assess*
Placement		*Incl. work-based learning and study that occurs overseas.*
Total hours	125	
ECTS ratio	25.00	

Project/placement activity

Is placement activity allowed?	No

Module delivery

Delivery mode	Taught/ Campus	Other	
Delivery term	Term 1	Other	

Ownership

Primary department	Electrical & Electronic Engineering
Additional teaching departments	
Delivery campus	South Kensington

Collaborative delivery

Collaborative delivery?	N

External institution	N/A
External department	N/A
External campus	N/A

Associated staff

Role	CID	Given name	Surname
Module Leader		Peter YK	Cheung

Learning and teaching

Module description

Learning outcomes	By the end of this module, students will be able to: • Describe the full-custom IC design flow including: system specification, circuit design, physical layout design, verification and preparation of tapeout. • Explain the trade-offs between the different IC design approaches including: full-custom, standard-cell and semi-custom, in terms of performance, area, power, cost, design effort and risk. • Understand key concepts in the fabrication process and the role that process design kits (PDKs) affect design constraints and the design flow. • Produce transistor-level circuits from a system-level specification for a specific application. • Design and simulate a moderately complex digital IC using industrial grade CAD tools. • Create layout-level designs of small circuits that adhere to DRC constraints using a suitable layout editing tool. • Perform logical and physical verification of the design using DRC, LVS, post-layout extraction, scan-insertion and automatic test pattern generation tools. • Generate a complete GDSII tapeout deck ready for silicon fabrication. • Verify that the fabricated chip is working.
Module content	Topics to covered: (see separte document for details) 1.VLSI design methodology overview 2.CMOS transistors characteristics, layout and rule contraints 3.Full-custom digital building blocks 4.Sequential digital circuit and datapath design 5.Hierarchical design and floorplanning 6.Placement, routing and extraction 7.Interconnection, clock tree and parasitics 8.Static and dynamic timing analysis 9.Design verification 10.Test insertion and generation, yield and manufacturability. 11.Tapeout preparation
Learning and Teaching Approach	While the underpinning concepts and methodology will be disseminated in 20 hours of lectures, most of the teaching and learning will happen in eight 3-hour supervised laboratory sessions. Five of the lab sessions will be supported by detail instructions in the form of experiment, the remaining lab sessions will be devoted to team-based design of an integration circuit for a given specification.

Assessment Strategy	The module will be assessed by four components: 1.Mid-term lab oral (10%) – serves as a milestone, feedback checkpoint and assessment on student's engagement in the lab up to that point. 2.End-of-term submission (50% split equally between team and individual marks) – a GitHub based submission which includes: 1) GDSII file; 2) full set of test vectors; 3) chip specification document; 4) team design report; 5) test procedure. 3.Written examination (30%) – tests student's knowledge and understanding. 4.Chip testing (10%)– when the fabricated chips are returned, test one of the return chips and write a short test report.
Feedback	Feedback will be continuously provided to student during the weekly 3-hours lab sessions which will be supervised by the module lead and GTAs, and through the two coursework assessment feedback reports.
Reading list	"CMOS VLSI Design: A Circuits and Systems Perspective", 4th Edition, ET Weste & David Harris, Pearon, 2015, ISBN: 9789332542884. "Digital Design and Computer Architecture, RISC-V Edition", Sarah Harris & David Harris, Morgan Kaufmann, 2021, ISBN: 978-0128200643.

Quality assurance

Date of first approval	June 2025
Date of last revision	June 2026
Date of this approval	
Module leader	Peter YK Cheung
Notes/ comments	

Office use only

QA Lead	
Department staff	
Date of collection	
Date exported	
Date imported	

Template version

Assessment details

Grading method	Numeric	Pass mark	50%

Assessments

Assessment type	Assessment description	Weighting	Pass mark	Must pass?
Examination	Exam (closed-book)	30%	50%	N
Practical	15-20 minutes individual lab oral on Lab 1 to 4	10%	50%	N
Coursework	GitHub Team report submission on chip design project	50%	50%	N
Coursework	Summer term effort in testing fabricated chip and produce short test report, or presentation on design and test plan in case the packaged chips are not returned in time.	10%	50%	N
		100%		