A Novel Vertical Solder Pump Structure for Through-Wafer Interconnects

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ABSTRACT

Through wafer interconnection is a critical technology for advanced packaging. Previously, we have proposed a solder pump technology which could complete the via filling through solder reflow. Here, an improved vertical solder-pump structure is presented and successfully demonstrated. This technology allows producing an arbitrary array of highly conductive vias in seconds.

INTRODUCTION

There is an increasing demand for low-cost, through-wafer interconnects in advanced packaging applications. Such interconnects currently use copper [1] or low-resistance polysilicon [2] as the conductive via material with main techniques for via filling being electroplating or chemical vapor deposition (CVD). We have developed a 'solder pump' technology for via filling, where molten solder is driven into the via hole using the capillary effect [3] in a single reflow step. This novel via-filling technique avoids the use of time-consuming electroplating or special wafers, and is compatible with conventional solder-based packaging. Here we propose and demonstrate a vertical configuration of the solder pump which can in seconds produce an arbitrary array of highly conductive vias.

STRUCTURE AND MECHANISM

The basic structure of a vertical solder pump is illustrated in Figure 1. Two dies are used to form the pump: a via die in which the interconnect will be formed, and a solder feed die which is separated from the via die using spacers. Both the via die and the feed die contain aligned through-wafer holes. Solder-wettable metal annular pads are patterned around the via hole on each side of the wafer. A vent die placed under the feed die provides support for the solder balls during loading, and acts as an air vent during reflow. Solder balls are placed into the aligned via and feed holes with a total solder volume sufficient to complete a conductive path through the entire thickness of the via die. The key requirement for a functional solder pump is that the feed-hole diameter has to be slightly smaller than the via-hole diameter.

The reflow of the solder in the vertical pump structure can be divided into two steps. The first step is the initial coalesence of the solder balls to form a contiguous volume of molten solder. The second step is the pumping of the solder from the feed hole to the via hole, driven by surface tension. Because the hole sidewalls are unwettable to solder, hemispherical surfaces are formed at the solder-air interface in both the via and the feed holes (see Figure 2). The pressure generated in the molten solder is given by $2\gamma/r$, where γ is the surface tension of the liquid solder and r is the radius of curvature of the hemispherical caps. For an unwettable sidewall r equals the hole radius. The driving pressure differential is given by [3]:

$$\Delta P = 2\gamma\left(1/r_{feed} - 1/r_{via}\right) \approx 2\gamma\Delta r / r_{ball}^2$$

Where Δr is the difference between the via and feed hole radii, with both holes slightly larger than the solder-ball radius r_{ball}. The solder will continue to reflow until it wets the upper metal pad metallisation with hemispherical caps formed on each side of the via hole (see Figure 3). The capillary forces completely dominate the effect of gravity for the solder balls used in this work. The pump can essentially be viewed as a mechanical structure that facilitates the conversion of surface-tension energy to potential energy to reform the solder as a through-wafer interconnect.

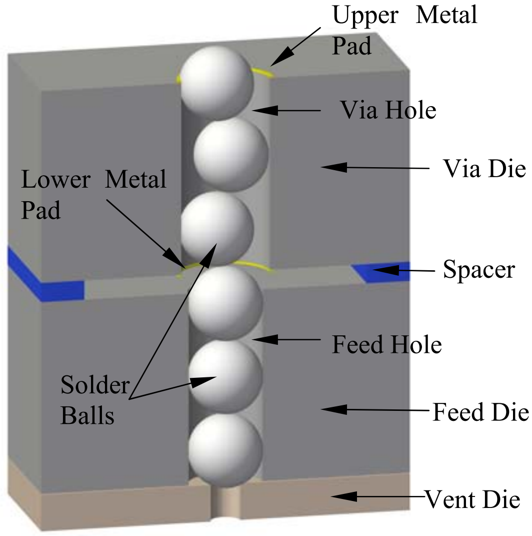

Figure 1 – Cross-sectional schematic of the vertical solder pump structure. The vent die allows (a) air to

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escape during solder reflow, and (b) is essential during solder ball loading.

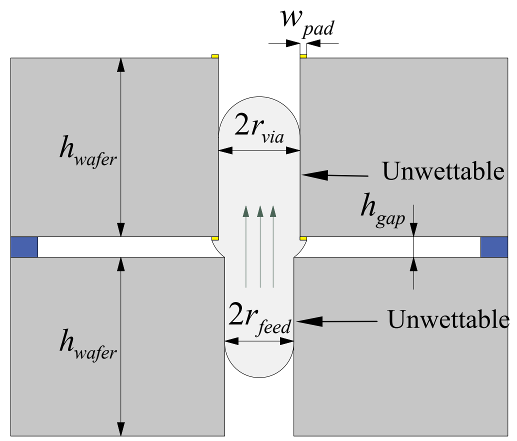


Figure 2 – Illustration of the geometrical parameters and working principle of a vertical solder pump. A difference in feed hole and via hole diameters leads to a pressure differential in the molten solder and solder pump action.

Table 1. Material properties of the used lead-free solder balls.

Solder Material Properties	Value
Density (ρ)	$7.31\times10^3\,kg/m^3$
Surface tension (γ)	$0.55\,N/m$
Viscosity (μ)	$0.012\ Pa\cdot s$ [5]

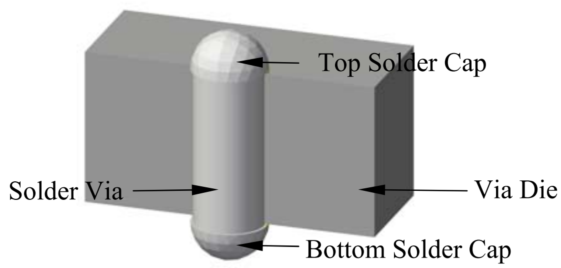


Figure 3 – Illustration of the final shape of the via hole solder column after successful reflow (Note: the feed/vent dies are no longer needed and are not shown here)

FABRICATION AND ASSEMBLY

The geometrical parameters of the demonstrator solder pumps are listed in Table 2. All the test structures were fabricated using standard 4”, $525\,\mu m$ thick, double-side polished silicon wafers. Figure 4 illustrates the fabrication process. All pump components here are realised on a single wafer with the holes produced by deep reactive-ion etching with subsequent surface isolation. Each test die contains an array of solder pumps. The standard annular pad metallisation is a sputtered metal multilayer of Cr (30nm) / Ni (250nm) / Au (100nm). Shadow-mask deposition inevitably leads to a thin metallisation of the via-hole sidewalls which does not affect the solder pump operation: the thin sidewall coating will either be simply dissolved by the relatively large amount of solder, or be wetted by the solder. Any wetting creates a negative pressure within the top surface of the molten solder hence assisting the pumping process.

Table 2 – Geometrical parameters of the fabricated solder pump test structures.

Geometrical Parameter	Symbol	Value (μm)
Solder Ball Radius	r_{ball}	150
Feed Hole Radius	r_{feed}	156
Via Hole Radius	r_{via}	170/175/180
Metal Pad Width	w_{pad}	50
Gap/Spacer Height	h_{gap}	50
Wafer Thickness	h_{wafer}	525

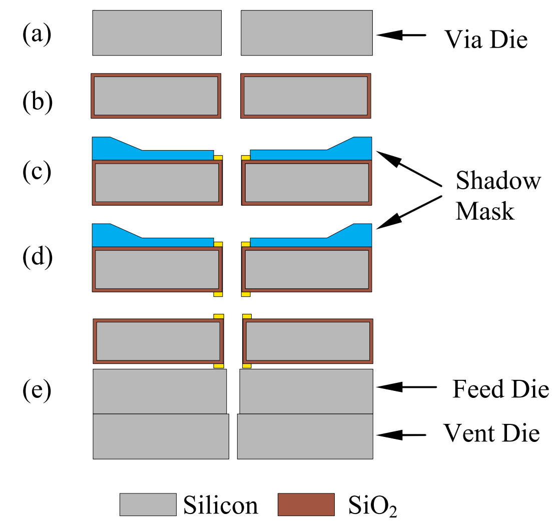
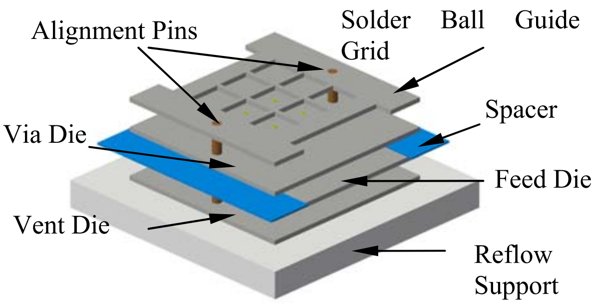
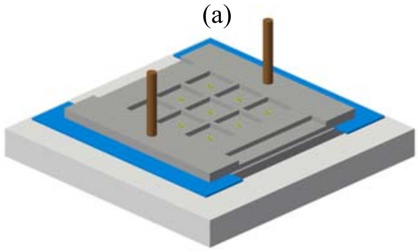


Figure 4 – Solder pump microfabrication process flow. All pump parts are machined from a single silicon wafer: (a) through-wafer hole etching and die separation by DRIE, (b) thermal oxidation (1 μm of SiO2) for electrical via isolation , (c) and (d) frontside/backside via metal pad deposition through silicon shadow masks, (e) pump assembly.

Figure 5 depicts the pump assembly. Alignment between the individual components is achieved with dowel pins. The solder balls are loaded into the through-wafer holes by placing the balls inside a guide grid and shaking the whole assembly. The actual solder reflow process has been described in detail in reference [3].



(a)

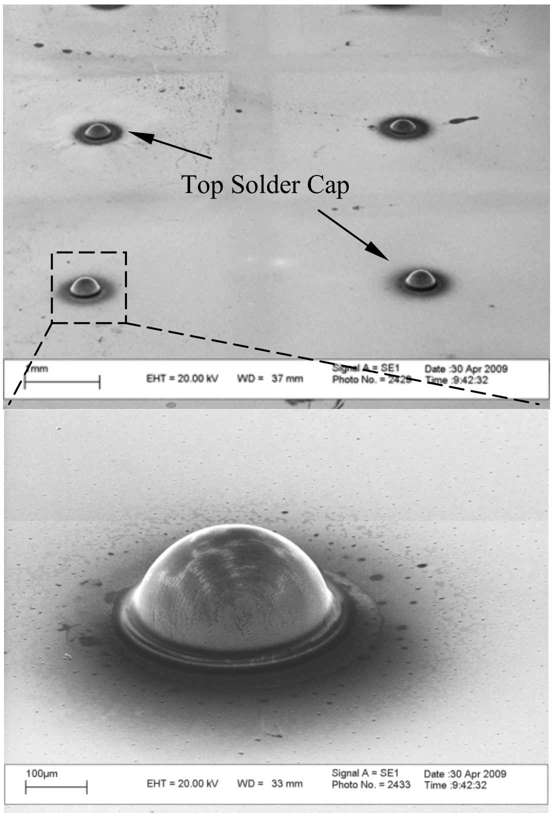


(b)

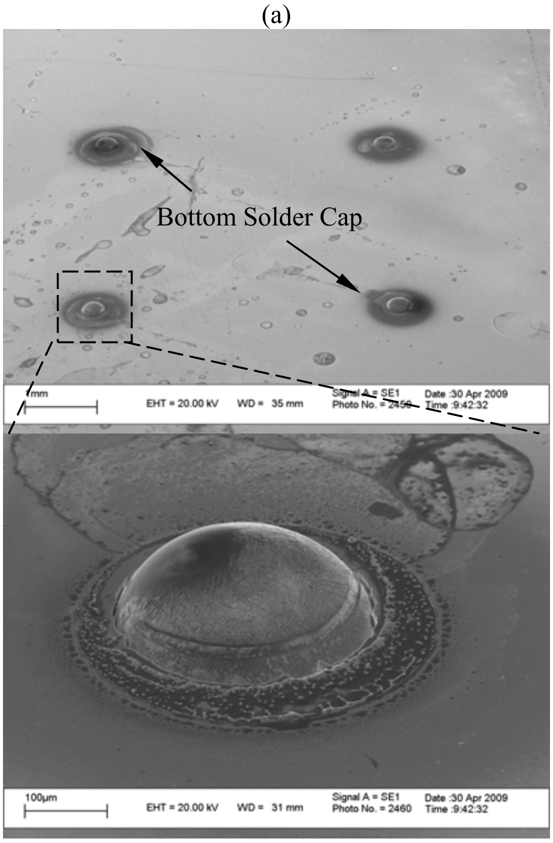
Figure 5 – Assembly of solder-pump TWI test structures for reflow: (a) explosion diagram showing all the individual pump and reflow support components, (b) fully assembled test die ready for solder reflow.

REFLOW RESULTS

Reflow is completed in a few seconds, consistent with a simple flow analysis of the pumping process. Figure 6 shows the front and backside of a via die after solder reflow. As it can be seen, solder bumps formed on both side of the via die. Figure 7 shows a cross section through a successfully formed solder via. The solder fills the through-wafer hole without voids. The solder balls in the feed die are completely transferred into the via die during the reflow.



(a)



(b)

Figure 6 – SEM pictures of four reflowed vertical solder pump test structures: (a) frontside view, (b) backside view of via die.

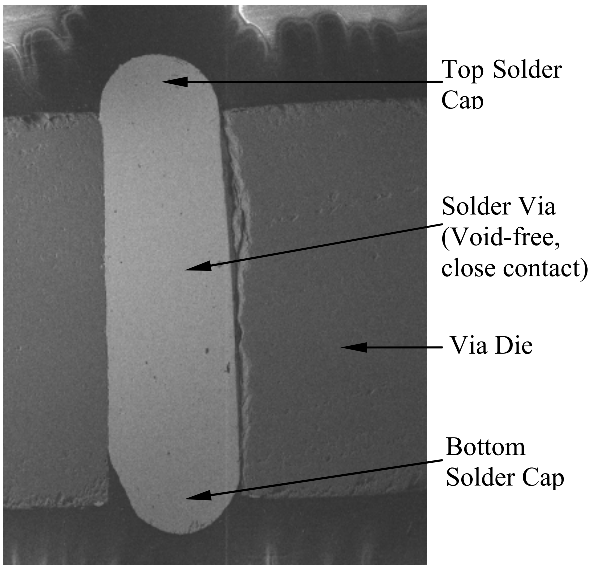


Figure 7 – Cross-sectional view of a low-resistance 'vertical solder-pump' solder interconnect (via die thickness of around 500 microns). Please note the void-free fill of the via through-hole and the hemispherical solder caps formed on each side of the via die during reflow.

CONCLUSIONS

A novel solder reflow-based interconnection technique has been demonstrated. First tests suggest that good reproducibility and reliability can be achieved. The feed die and vent die are left with no solder residue and can be used repeatedly. The vertical pump geometry can be scaled down further using smaller solder balls. The solder-pump technique has several advantages over conventional through-wafer-interconnect methods: (a) there is no requirement for any special wafers; (b) it is a fast process - while electroplating or CVD can take several hours to fill a via, the reflow of the solder pump only takes seconds; (c) it allows a flexible configuration of vias to meet the requirements of various applications; (d) it produces low resistivity vias. The technique is suitable for MEMS packaging, wafer-level packaging and surface mounting.

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