A 2.7 μW/MIPS, 0.88 GOPS/mm² Distributed Processor for Implantable Brain Machine Interfaces

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Features:
- 2.7 μW/MIPS custom processing unit at 20MHz with 12b precision instrumentation analogue
- Scalable pipeline architecture with 32kb on-chip eDRAM memory and power management
- 1k fully reconfigurable instruction buffer for filtering, calibration, classification, compression
- 64 channel system in 0.18 CMOS uses 2.64 mm² active area and 1.7mW

Analogue Systems

Digital Systems

Fully integrated brain machine interfaces substantially improve efficacy. This requires the development of distributed & adaptive processing.

DSP for Spike Sorting and Neural Recording

Principle Motivation
- Ultra power efficient
- Highly reconfigurable
- DSP for 1k Channels

Technology Scaling for Noise-Limited Systems

Technology[mm]

R_re(Blue) R_PA(Green)

SNR

R_re(Blue) R_PA(Green)

Technology[mm]

Table 1: Performance comparison with state-of-the-art DSP ASICs.

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<tbody>
<tr>
<td>System</td>
<td>Neural</td>
<td>Imager</td>
<td>Imager</td>
<td>Neural</td>
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<tr>
<td>Scaling</td>
<td>Fine</td>
<td>Coarse</td>
<td>Coarse</td>
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<td>Tech. [nm]</td>
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<td>65</td>
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<td>64</td>
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<td>Sys. Power [mA]</td>
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<td>Tile Memory [kb]</td>
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<td>P Merit [GOPS/mW]</td>
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<td>A Merit [GOPS/mm²]</td>
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</table>

Summary

 Pipelined Architecture
- Arbitrary # Recordings
- Low speed I/O & less off-chip telemetry
- Fully integrated SOC
- Reduced PCB footprint

Wideband Neural Recording
- 100KSa/s @ 12bit for LFP & EAP signals
- Minimal analogue distortion (50dB THD)

8b RISK µC unit
- 20MHz operation with 1kB in channel memory
- 1024 instructions per sample
- Immediate processing enables adaptive filters

Results

Fabricated with 6 Metal 0.18 μm CMOS technology (AM5/IBM18A6/75F)
Die size is 6.2mm² including test circuits and peripheral pad ring.

References