# Autonomous SoC for Neural Local Field Potential Recording in mm-Scale Wireless Implants

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## Summary
- Distributed architecture for 100s of sub-dural implants
- Wireless neural recording SoC with self-regulating supply
- Fully integrated system using only one external coil
- 92μW power budget while recording from 8 electrodes
- 0.1 - 825Hz Signal Bandwidth with 1.77μVrms Noise Figure
- Tracking 2nd Order ΔΣ topology for AFE with >100Ω $R_{in}$
- >66dB of dynamic range with no in-band noise corner

## Introduction
Next generation brain machine interfaces fundamentally need to improve the information transfer rate and chronic consistency when observing neural activity over a long period of time. Towards this aim, the ENGINI project presents a novel System-on-Chip (SoC) for mm-scale wireless neural recording node that can be implanted in a distributed fashion.

**ENGINI Challenges:**
- Improve the decoding capacity of BMIs and record from multiple brain structures
- Ensure chronic stability and long-term reliability of the implanted devices
- Achieve complete wireless power delivery and data telemetry
- Increase the energy efficiency of the complete system to enable high data throughput

## System Block Diagram

![System Block Diagram](image)

## System Specifications
- **Features**
  - Low-Cost 0.25μm 2P4M CMOS Design
  - 0.23mm² AFE+DSP core per channel
  - NEF of 2.3 and PEF of 8.1
  - >200mV electrode offset tolerance and ±10mVp input range for 10 - 900kHz
  - Supply noise rejection with 90dB PSRR
  - Delta modulation of near-DC signals for increased dynamic range
  - 210kHz/LSK data rate from I²F band

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* Based on measured results and preliminary benching testing.

## Instrumentation Front End
- Compact configuration with high sensitivity and reconfigurability of $f_{ref}$
- Intensive to process variation w.r.t $V_{ref}$, $V_{DD}$, $G_{sw}$, $R_{in}$
- Applicable to both synchronous and asynchronous systems
- Will scale improved efficiency and size with more advanced CMOS

## Telemetry & Bias Circuits
- **Vref Regulation & Impedance control**
  - Bb Capacitor array tunes the LC tank
  - Impedance mismatch controlled VDD
  - without inducing resistive losses on-chip
  - Unique FM Mask for LSK data to identify multiple probes operating simultaneously

## ADC Band-gap Reference Circuit
- Low $\alpha$, High PSRR, 1.2V reference from $V_{ref}$
- $<1$V Supply voltage operation
- 1V, 1.3V, 1.5V $V_{ref}$ level indicators for FSM
- 140nA bias current for each sensor FE

References: