Integrated Devices for Micro-Packgage Integrity Monitoring in mm-Scale Neural Implants

Federico Mazza1, Yan Liu1, Nick Donaldson2, and Timothy G. Constandinou1
1Centre for Bio-Innovative Technology, EEE Department, Imperial College London, South Kensington Campus, London SW7 2BT, UK
2Department of Medical Physics and Bioengineering, University College London, WC1E 6BT, UK

OVERVIEW

• Latest advancements in technology allow for a next generation of smaller, smarter implantable biomedical devices capable of extracting information from the body’s internal bio-signals.

• Great technological challenge in providing a hermetic packaging to implantable devices, to avoid any undesired interaction with tissue while allowing functional interfacing. Scaling down implant sizes to the sub-millimeter domain precludes the use of standard manufacturing techniques and test methods.

• This work presents a novel concept for in situ instrumentation for monitoring water penetration in silicon based micro-packages. The proposed circuits are integrated within the same active CMOS substrate and do not require post-processing. They can prove to be a valuable way to monitor over time the integrity of the device, as well as provide insight on the mechanisms of moisture penetration in a CMOS stack.

HERMETICITY TESTING OF MICRO-PACKAGES

Current methods for testing the hermeticity of electronic packages and MEMS can be grouped in the following categories:

• Leak rate tests: helium leak test (industry standard MIL-STD-883, Method 1014.10), radioisotope leak test, cumulative helium leak detection (CHELD).

• Spectrometry tests: Fourier transmission infrared spectrometry (FTIR), Raman spectroscopy.

• Deformation tests: lid deflection optical test.

• In situ tests: resonator’s Q-factor, copper test patterns, integrated pressure or humidity sensor.

Most of the above test methods are not sensitive enough for cavity sizes below 1mm², and some can only be performed during the fabrication of the device.

In the case of implantable devices safety is of primary importance; in the event of a functional failure, implants should not pose a health risk for the patients, and they must remain safe at least in the short term. In situ methods are therefore preferred, since they allow for monitoring of hermeticity over time.

HUMIDITY INGRESS IN SILICON-BASED MICRO-PACKAGES

Miniaturation of biomedical implants can be achieved using materials and techniques belonging to the electronics micro-fabrication domain. This also allows for the integration of active circuits on the same substrate that constitutes the package. The use of active CMOS or silicon interposers as R&D provides improved connectivity and can increase the number of feed-throughs, but poses new challenges for hermeticity.

Moisture can penetrate in multiple ways inside the micro-package:

1. Cracks in the metal seal ring, due to defects during fabrication or corrosion;
2. Improper adhesion of TSV;
3. Infiltration at the interface between different oxide and metal layers in a CMOS stack;
4. Diffusion within the bulk of intrinsic silicon or SiOx.

The last two cases may not cause any build up of moisture inside the cavity, but can lead to the corrosion of the metal tracks and compromise proper device operation. An in situ sensor is not sufficient, and specific structures are required.

INTER-LAYER INFILTRATION

• Fabrication defects or stress induced cracks can allow moisture to penetrate at the interface between the different silicon dioxide inter-layer dielectrics (ILDs).

• Moisture eventually reaches the outer metal traces and shorts them with the die seal ring.

• A differential impedance measurement along the horizontal direction is performed, comparing the outer parasitic impedances Z1-out and Z2-out with the inner parasitic impedances Z1-in and Z2-in.

The circuit used for the measurement is composed of two stages:

1. Discrete time differential trans-impedance amplifier (TIA) with the inputs connected to the inner and outer metal tracks.

2. Switched capacitor inverting amplifier with CDS for offset correction.

Signal bandwidth is near DC with magnitude in the range of 1 to 100pA. A smaller amplification bandwidth is preferred to reduce the noise bandwidth and aliasing and is achieved using a sampling frequency lower than the corner frequency of the flicker noise.

A larger PMOS pair (600µm x 1µm) is used in the first stage folded cascode amplifier, to minimize the flicker noise in the sampling/harmonics, and 1pF capacitors are used as feedback capacitors to minimize the effect of input parasitic capacitance for noise reduction.

Total power consumption is 4.76µA at 3V power supply.

REFERENCES

