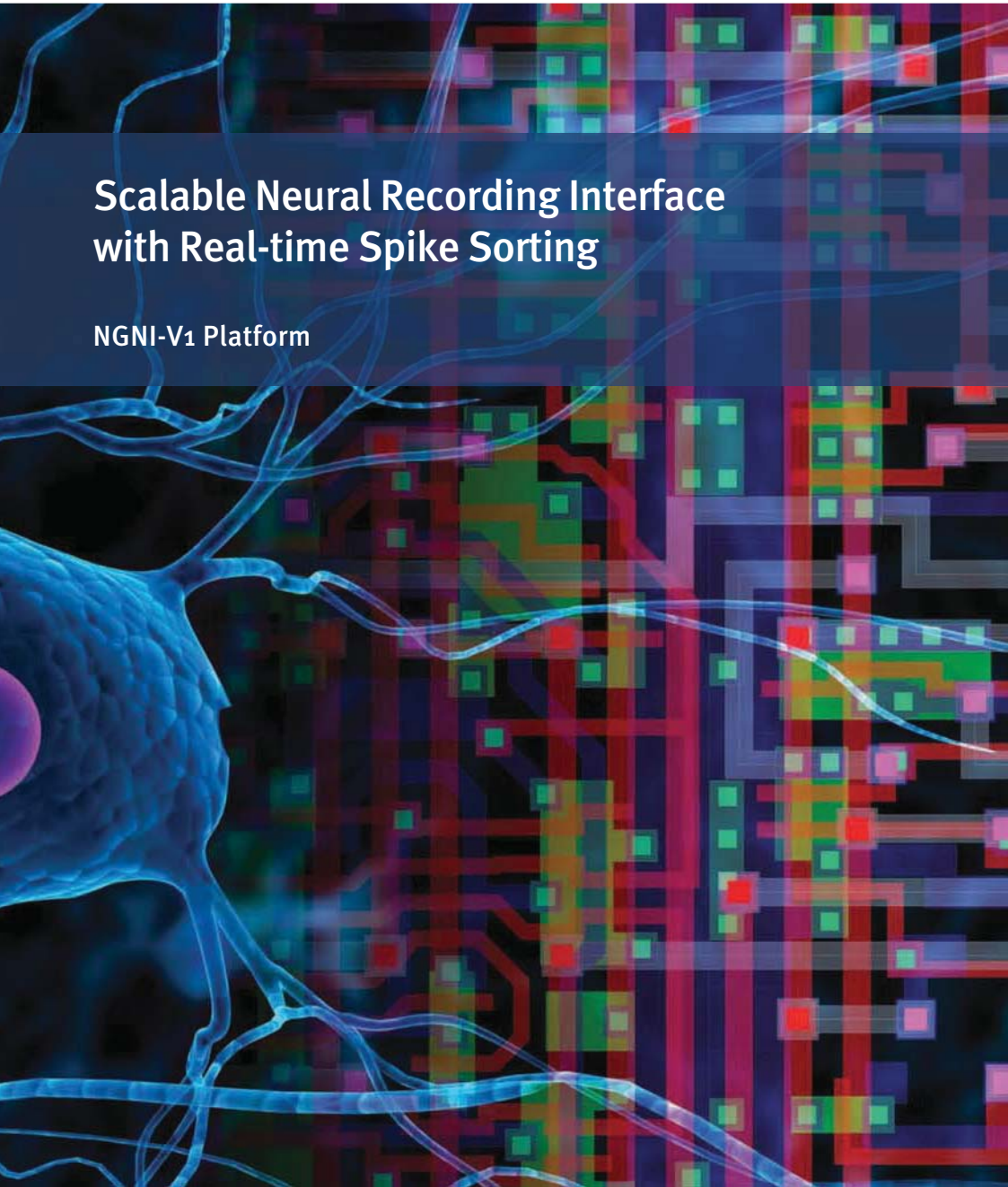
NGNI | Imperial College London

Newcastle University

UNIVERSITY OF LEICESTER



Scalable Neural Recording Interface with Real-time Spike Sorting

NGNI-V1 Platform

OVERVIEW

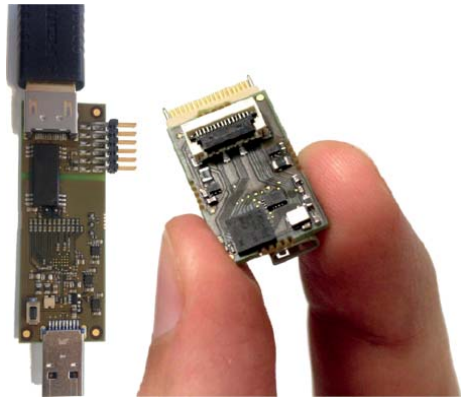
Spike Sorting On-Node and Real-Time

Spike Sorting is the process of deinterleaving a recorded neural signal in order to determine the firing patters of individual neurons from the aggregate spike stream.

The NGNI platform is an end-to-end solution for on-node, real-time spike sorting. By using a compact, onboard (template based) spike sorting engine, together with offline training (WaveClus-based), a low power real-time solution is achievvable

The main components of the NGNI-v1 module are an Intan RHD2132 neural amplifier and a low power Igloo FPGA. The Intan RHD2132 contains 32 low noise amplifiers and bandpass filters multiplexed into a single 16-bit ADC for neural signal filtering, amplification & digitisation. The low power Igloo FPGA performs spike sorting and communication. It also includes a standard pitch header (for connection to electrodes) and a micro HDMI connector for digital communication (and if desired external power). If used in conjunction with the NGNI USBridge motherboards this power can safely be sourced from USB and can allow for limited scalability (160 channels).

The system operates in a two stage process that leverages the high performance unsupervised spike train clustering and deinterleaving capability of a proprietary WaveClus implementation. In the first stage the NGNI-v1 is configured to send raw data to a computer for offline analysis with WaveClus. The generated templates (up to 4 per channel) are then uploaded to the NGNI-v1 which implements a computationally efficient algorithm to perform real-time spike sorting. The spike sorted data is transmitted via the NGNI USBridge (over SPI and then USB) to a PC. A GUI is provided for data visualisation and system configuration.



NGNI V1 platform showing 32-channel headstage and USB3.0 SS bridge.

Software platform for configuration and real-time visualization of neural recording and spike sorting.

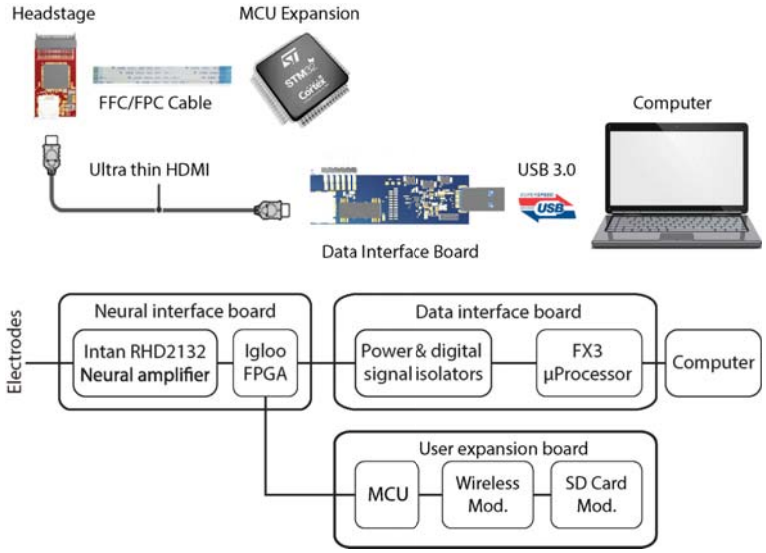
FEATURES

- 32-channel neural recording/streaming
- On-node, realtime template-based spike sorting
- Proprietary template building engine (based on WaveClus)
- Onboard template memory, 18.4kbit (4 templates per channel)
- Low latency (0.3ms) SPI output
- Low output datarate for wireless communication

APPLICATIONS

- Signal acquisition systems for electrophysiology
- Large-scale recording applications (multi-probe, multi-channel)
- Realtime brain machine interface applications
- Closed loop low-latency biofeedback

NGNI V1 PLATFORM ARCHITECTURE



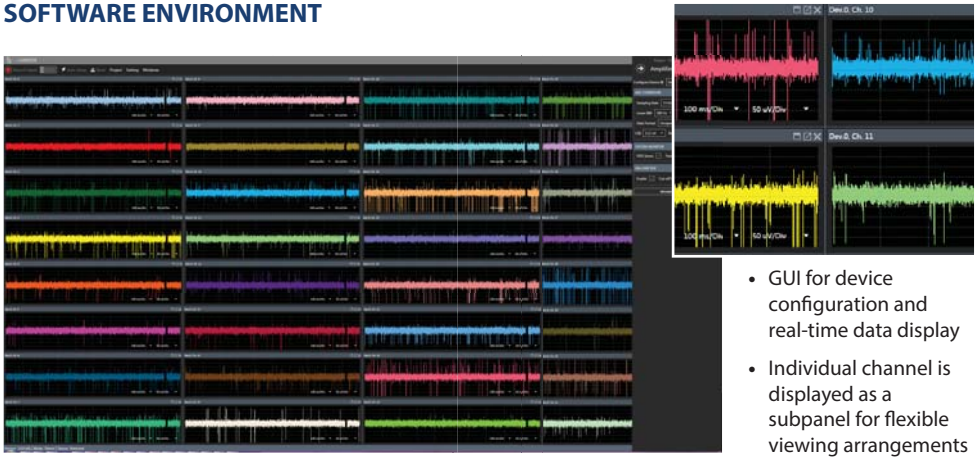
This is the first compact design targeted at *in-vivo* application. Size and weight have been reduced while extra functionality has been included such as:

- An extra SPI link enables MCU expansion and standalone operation or wireless connection.
- Simultaneous matching events and raw signal output
- CMOS outputs for matching event on selected templates

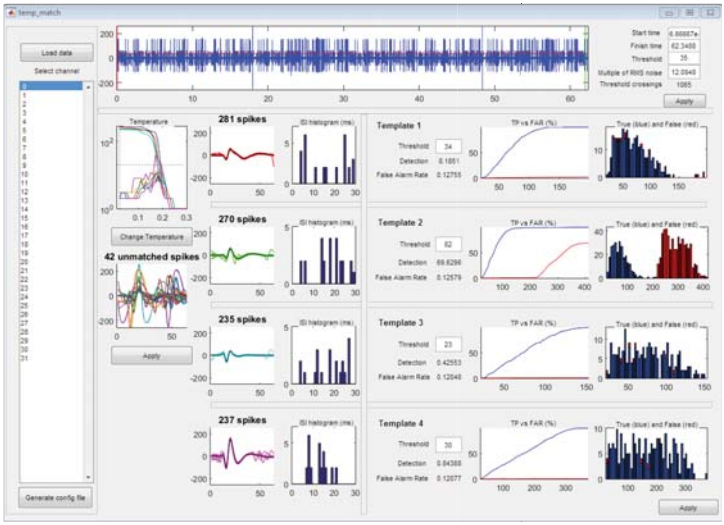
ELECTRICAL SPECIFICATION

Power supply	3.13-5.5 V	CMRR	82 dB
Amplifier differential gain	192	PSRR	75 dB
Sampling rate	15 kHz	THD (@1kHz, 4mVpp, 0.1-10kHz)	0.1 %
ADC resolution	9-bit	Amplifier crosstalk	-68 dB
Low-frequency 3dB cut-off	0.02-500 Hz	Amplifier input capacitance	12 pF
High-frequency 3dB cut-off	100-20 kHz	Amplifier reference Input capacitance	325 pF
Amplifier AC input range	±6.4 mV	Amplifier Input Impedance	13 MΩ @ 1kHz
Amplifier DC input range	± 0.4 mV	Amplifier reference Input impedance	0.5 MΩ @ 1kHz
Amplifier input-referred offset voltage	< ±100 µV	Amplifier input-referred noise	2.4 µVrms

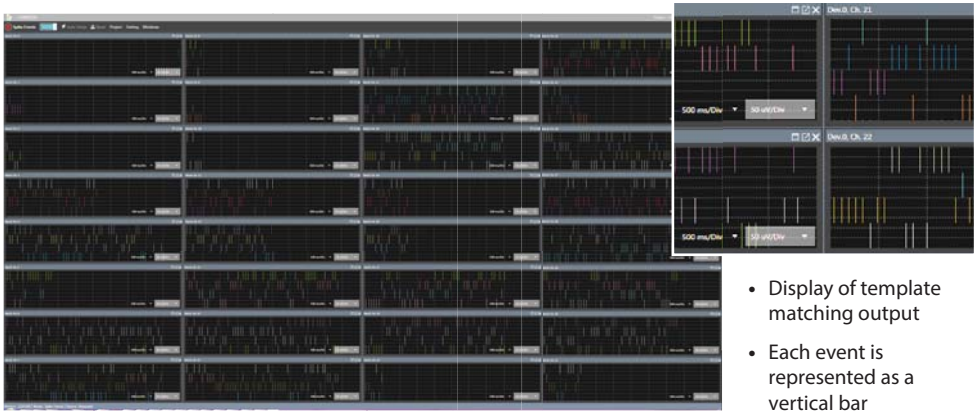
SOFTWARE ENVIRONMENT



- GUI for device configuration and real-time data display
- Individual channel is displayed as a subpanel for flexible viewing arrangements



- MATLAB Based GUI for offline clustering
- Template and configurations are generated with WaveClus



- Display of template matching output
- Each event is represented as a vertical bar

EXPERIMENTAL PROCESS FLOW

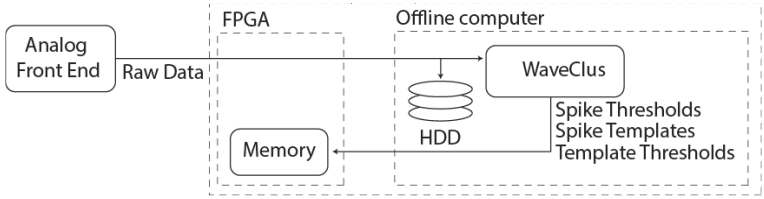
Learning phase — Raw signal output

On startup an initial configuration is loaded from a PC based configuration GUI. The raw neural signal is then digitised by the analogue front-end (currently Intan RHD2132) and passes directly through the FPGA to the computer to be stored.

A Matlab GUI is provided for offline clustering. The underlying method is based on WaveClus. The GUI allows the user to visualize different templates and associated spikes together with accuracy and false alarm rate estimation. The user can automatically generate templates for all 32 channels or manually do it on selected channels. The following parameters will be uploaded after template generation:

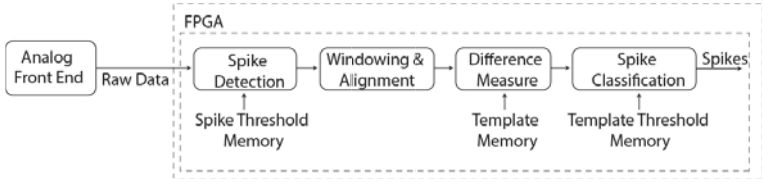
- Spike detection thresholds (per channel)
- Spike templates (4 per channel), 16x 9-bit samples per template.
- Template matching thresholds (per channel)

The configuration will be saved in a binary file and uploaded by the configuration GUI to the FPGA. Alternative clustering methods or software can be used to generate the required templates/configuration data.



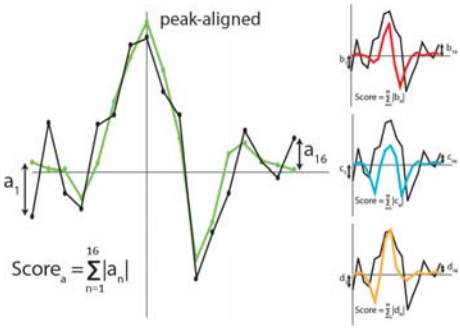
Autonomous phase — Spike sorting output

Once the FPGA has valid templates & thresholds it can be put into template matching mode. In this mode the FPGA evaluates all the incoming data against assigned templates using sum of absolute distance method. The best matching template with a score below the programmed threshold would signal a matching event to the computer. This matching event would report the matching time, channel number and template ID.



TEMPLATE-BASED SPIKE SORTING

Similarity Quantifier



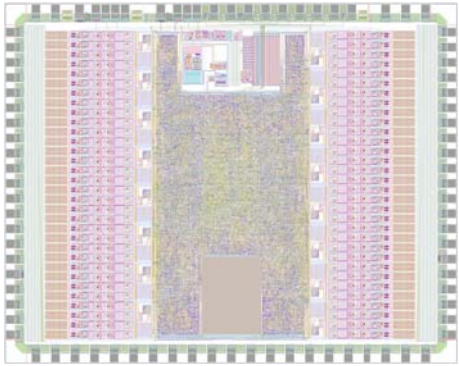
Distance based template matching method. Colour traces are templates. Black traces are input signals. The score is the sum of distances between signals and templates. The matching template achieves the lowest score that is below a user set threshold.

Sampling rate	15 kSample/s
Word length	9-bit
Spike detection	Single Threshold
Threshold range	9-bit
Classification method	Template matching
Alignment method	Peak
Template length	16 samples (1ms)
Template align offset	5 samples (from abs.)
Distance measure	Sum of abs. difference
Template/channel	4
FPGA family	Igloo Nano
Total memory	18.4 kbit

DEVELOPMENT ROADMAP

Upcoming Features (in development):

- Standalone recording solution with wireless access
- LFP and spike recording over the same area
- Thousands of channels recording and sorting
- Single-chip Application Specific Integrated Circuit (ASIC) solution



64-channel ultra-low power NGNI V2 chip (in fab)

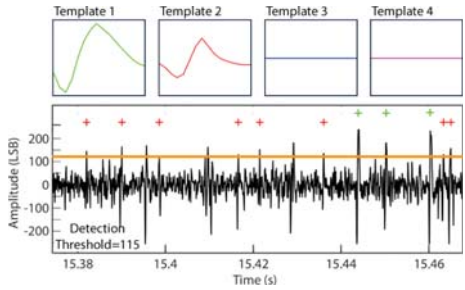
Version	Features	Power (mW)	Dimensions and Weight	Ch. per module (max. # of mod.)
NGNI-V1 (Q2 2016) Evaluation system available soon	AP, SS, SPI, USB3	34	26mm x 14mm x 4mm, ~2g	32/64/96 (x1)
NGNI-V2 (Q4 2016)	AP, LFP, SS, SPI, USB3	~15	26mm x 14mm x 6mm, ~3g	64/128/192 (x8)

AP = "raw" extracellular action potential recording, LFP = "raw" local field potential recording,
SS = Realtime spike sorting, SPI= Local, auxillary SPI output, USB3= Host interface using USB3 bridge

PRELIMINARY *IN-VIVO* RECORDING AND SPIKE SORTING RESULTS

Experimental measurements taken on NHP with tungsten microwire electrodes implanted in Motor and Premotor Cortex. Front-end configured for a signal band of 300Hz-3kHz with digital high pass filter set at 318Hz.

Data plotted using Matlab shown below.



Different unit events (classified spikes) indicated by coloured crosses. Associated templates shown in sub-plots above.

Noise level recorded at 12.7 µV (limited by experimental measurement, not platform).

References

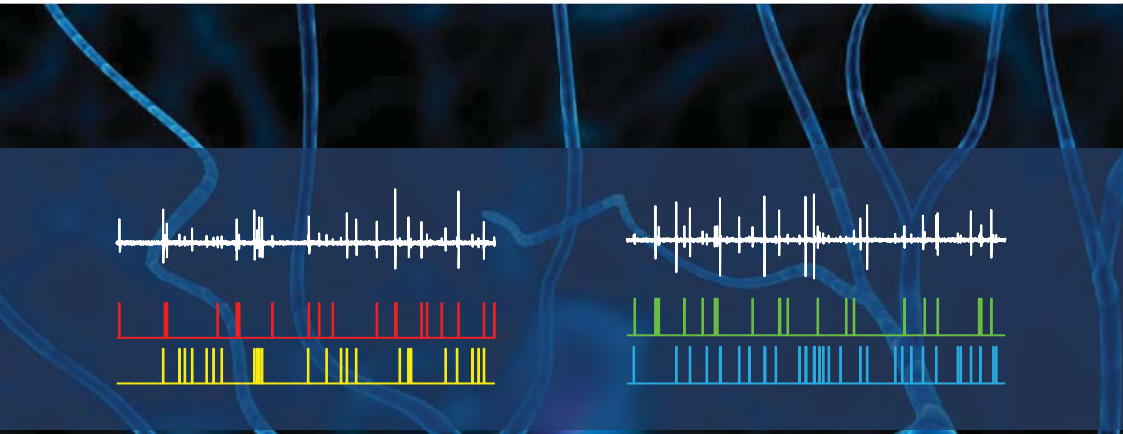
- Williams I, Luan S, Jackson A and Constandinou TG. "Live demonstration: A scalable 32-channel neural recording and real-time FPGA based spike sorting system." *In 2015 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, pp. 1-5. 2015.
- Jackson A, Constandinou TG, Eftekhar A, Quiroga RQ and Navajas JA. "System for a Brain-Computer Interface", PCT WO2015114347, 2015.
- Barsakcioglu DY, Liu Y, Bhunjun P, Navajas J, Eftekhar A, Jackson A, Quiroga RQ, and Constandinou TG. "An analogue front-end model for developing neural spike sorting systems." *IEEE Transactions on Biomedical Circuits and Systems*, Vol. 8, No. 2, pp. 216-227, 2014.
- Navajas J, Barsakcioglu DY, Eftekhar A, Jackson A, Constandinou TG, and Quiroga RQ. "Minimum require ments for accurate and efficient real-time on-chip spike sorting." *Journal of Neuroscience Methods*, Vol. 230, pp. 51-64, 2014.
- Barsakcioglu DY, Eftekhar A, and Constandinou TG. "Design optimisation of front-end neural interfaces for spike sorting systems." *In 2013 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 2501-2504, 2013.
- Quiroga RQ, Nadasdy Z, and Ben-Shaul Y. "Unsupervised spike detection and sorting with wavelets and superparamagnetic clustering." *Neural computation*, Vol. 16, No. 8, pp. 1661-1687, 2004.

Supported by:

EPSRC

EP/I000569/1
EP/H051570/1
EP/H051651/1
EP/K015060/1

Engineering and Physical Sciences Research Council



For further information please contact:

Timothy Constandinou, PhD
Dept. of Electrical & Electronic Engineering, Imperial College London
South Kensington Campus, London SW7 2AZ, UK
Tel: +44 (0)20 7594 0790 | Fax: +44 (0)20 7594 0704
Email: t.constandinou@imperial.ac.uk
Web: http://www.imperial.ac.uk/people/t.constandinou
http://www.imperial.ac.uk/neural-interfaces

Andrew Jackson, PhD
Institute of Neuroscience, Henry Wellcome Building, Medical School,
Newcastle University, Newcastle-upon-Tyne NE2 4HH, UK
Tel: +44 (0)191 208 6685
Email: andrew.jackson@newcastle.ac.uk
Web: http://research.ncl.ac.uk/jacksonlab/

Rodrigo Quian Quiroga, PhD
Centre for Systems Neuroscience, University of Leicester
9 Salisbury Road, Leicester LE1 7QR, UK
Tel: +44 (0)116 252 3249
Email: rqqg1@leicester.ac.uk
Web: http://www2.le.ac.uk/centres/csn/people-1/Rodrigo