CURRICULUM VITAE

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DATE OF BIRTH: 7 February 1969

NATIONALITY: British

ACADEMIC AND RESEARCH APPOINTMENTS:

1. Professor of Quantum Nanoelectronics
Optical and Semiconductor Devices Group, Department of Electrical and Electronic Engineering, Imperial College London

Reader: September 2015 –2023, Senior Lecturer: April 2007 – August 2015.

A. Principle Area of Research:
My research interests include quantum nanoelectronics, single-atom devices, semiconductor nanodevices, condensed matter physics, energy scavenging, nanostructures and nanofabrication. A major theme in my work has been the development of 'beyond CMOS' quantum electronic devices with dimensions reduced to the ~1 nm scale, for large-scale, practical application. This research addresses significant present-day problems in the further development of classical semiconductor transistors, which may potentially end Moore's Law. I am addressing these issues using a comprehensive approach, from basic physics to device applications. Other significant areas of research include energy scavenging in semiconductors, nanofabrication methods down to the single atom scale, and the physics of nanocrystals and nanowires.

B. Research Grants:

1. 'Room-Temperature Single Atom Silicon Quantum Electronics' (EPSRC, UK)
   May 2021 – November 2024, Principle Investigator
   Project consortium with UCL, to develop single atom quantum transistors, sensors, memory and logic circuits, capable of room-temperature operation. Imperial College is the lead institution. The grant provides 1 PDRA at Imperial. Imperial / Consortium budgets: £694,633/£1.26M.

2. 'Atomic resolution STEM characterization and in situ electron transport measurements of room-temperature single-electron transistors' (Oak Ridge National Laboratory, USA)
   March 2020 – March 2022, Principle Overseas Investigator
   This project is exploring *in situ* TEM measurements of single-atom and semiconductor nanocrystal quantum transistors. The grant provides time, facilities and consumables for two personnel at Oak Ridge National Laboratory.

3. 'Single Nanometer Manufacturing for beyond CMOS devices' (EU FP7 Programme)
   January 2013 – March 2017, Principle Investigator
   Large Integrated Project with 15 consortium partners, investigating ~5 nm scale electronic devices fabricated using scanning probe and electron beam lithography. 3 PDRAs and 1 RA/PhD research student worked on the project. I also managed the Devices Working

Group within Consortium (ICL, EPFL, CSIC Barcelona). Imperial / Consortium budgets: £566,577/€11.7M.

4. 'Si/SiGe Nanowire Arrays for Thermoelectricity', (EoN Int. Research Initiative)
   December 2008 – November 2011, Co-Investigator
   Project investigated the thermoelectric performance of large arrays of Si nanowires. 1 PDRA and 1 PhD research student worked on the project. Budget: £451,222.

5. 'Solution Oriented Research for Science and Technology' (Japan Science and Technology)
   June 2007 – October 2009, Principle Investigator
   The project investigated electronic transport in Si nanocrystals and nanowires. Prior to this, the project was at the Dept. of Engineering, University of Cambridge (Oct. 2004 – May 2007), where I was the co-investigator. Budget: £280,000.

C. Research Collaborations:

1. EU: Universities: Ilmenau, Tübingen, Bayreuth, Delft, EPFL, CSIC Barcelona. Industrial: IBM Zurich, EVG group, IMEC, Swiss Litho, VSL Dutch Metrology.
2. Japan: Tokyo Institute of Technology, Japan Advanced Institute of Science and Technology, Tokyo University of Agriculture and Technology, Nagoya University, Hitachi Central Research Laboratory.
3. UK: University College London, University of Cambridge, University of Southampton, A-Modelling Solutions, Hitachi Cambridge Laboratory, Oxford Instruments.
4. USA: Oak Ridge National Laboratory.

D. Undergraduate and Postgraduate Teaching:

1. EE1-02 Digital Electronics 1 (Oct. 2009 – Sept. 2021).
   1st Year, 20 Lectures and problem classes. 160 – 200 students per year. ~95% positive student feedback (responses in top 2, 'Definitely agree', 'Agree', of 5 categories).
2. ELEC60029 Semiconductor Devices, (October 2021 - present)
   3rd Year, 20 Lectures, ~20 students per year.
3. EE4-44/ EE9-AO11 MEMS and Nanotechnology (Jan. 2009 – present).
   4th Year, I lecture nanotechnology part, 10 lectures. ~20 students per year. 86% positive student feedback (responses in top 2, 'Definitely agree', 'Agree', of 5 categories).
4. EE1-03 Semiconductor Devices (2007 – 2008). Lectures and problem classes.
5. Laboratory Staff Demonstrator, 1st and 2nd year laboratories.
   1st year Laboratory: 2007 – 2009, and 2013 – present, 2nd year laboratory: 2010 – 2012.
6. 1st Year and 3rd Year Undergraduate Tutor (2007 – 2010, and from Oct. 2014).
7. MEng and BEng Final Year project supervisions.
8. Industrial Placement project supervisor.

E. Administration:

1. Department Post Graduate Scholarship Committee (Oct. 2020 - present).
2. Undergraduate Admissions Tutor (Oct 2013 – Sept. 2020).
   Responsible for UG admissions. This comprises interviews and their organisation, talks to candidates/parents, admission offers, open days, membership of University Admissions Committee.
3. Deputy Admissions Tutor (Oct. 2012 – September 2013).
4. Deputy Director Undergraduate Studies (2010 – 2012).
   Supported Director of UG studies. This comprised attendance at Faculty Teaching Committee / Eng. Studies Committee if DUGS unavailable, support with UG prizes, timetables, graduate teaching assistants, contribution to quality assurance exercise.
5. Deputy Head, Optical and Semiconductor Devices Group (2020 - present).
   I support group head in management of cleanroom and laboratory facilities.
6. Chemical Safety Officer, Department of Electrical and Electronic Engineering.

F. PhD students

1. Imperial College (2008 – present):

Supervised to completion 5 PhD students. 2 current PhD students
2. University of Cambridge (1998 – 2006):
Supervised to completion 4 PhD students (of whom one shared).

G. Other professional activities:

1. University of Edinburgh External Examiner (Oct. 2016 – Sept. 2020).
I served as external examiner for the UG courses of the Dept. of Electronic and Electrical Engineering. This involved inspection of exam papers and scripts, projects, course organisation, attending examiner's meetings, and providing an annual examiner's report.
2. Organised the Micro and Nano Engineering (MNE) 2013 conference (Programme Chair).
16 – 19th September 2013, Imperial College.
679 participants, 569 papers presented in four parallel sessions, supported by 7 sponsors and 33 exhibitors.
3. Editorial Boards:
(i) Editorial Board of Microelectronics Engineering (Elsevier) Journal (Nov. 2011 – present).
(ii) Guest Editor, Microelectronics Engineering, Special Issue on Nanolithography. Issue completed Sept. 2014.
(iii) Review Editorial Board of Frontiers in Electronics (2021 - present)
4. External Committees:
(i) International Steering Committee, Micro and Nanoengineering (MNE) Conference Series (Jan 2008 - 2018). (ii) MNE2013 Organising Committee. (iii) Board Member, International Micro and Nano Engineering Society (iMNES), (2019 – present).
5. Fellow of the Institute of Physics (07/2021 – present).
6. Fellow of the Institution of Engineering and Technology IET (11/2021 - present)
7. Member of the Institute of Physics (05/2007 – 06/2021) and the IET (05/2008 - present).
8. Project proposal reviews for EPSRC, EU Marie Curie programme, and Leverhulme Trust. I also act as reviewer for journals of the American Inst. of Physics, Institute of Physics, IEEE and Elsevier.

2. Research Associate (2004 – 2007)

Electronic Devices and Materials Group, Department of Engineering, University of Cambridge

Co-investigator for the 'SORST' project (Japan Science and Technology). See Research Grants, Sec. 1-B, above).

3. Research Associate (1997 – 2004)

Microelectronics Research Centre, Department of Physics, University of Cambridge

A. Research Grants

'Coulomb Blockade Logic' (EPSRC)
March 2001 – February 2004.
I wrote, prepared and ran this grant. At that time, Univ. of Cambridge rules did not allow me to act as P.I., who was the Head of Group. The project demonstrated low-power logic switching elements based on charge packets only 1-2 electrons in size. Supervised 1 PDRA and 1 PhD student. Budget: £307,180. Project reviewed as 'tending to outstanding'.

B. Other Research:

1. CREST 'Neo-Silicon' project, Japan Science and Technology (2000 – 2004).
Responsible for running this project. Work investigated single electron and quantum dot devices using Si nanocrystals. Supervised 1 PDRA and 2 PhD students.
2. 'Fabrication of Single Electron Memories' project, EU ESPRIT (1997 – 1999).
I worked as a PDRA on this project. Developed CMOS compatible single-electron memory arrays.

C. Teaching:

1. Lecturer, MPhil in Microelectronics Engineering and Semiconductor Physics (1999 – 2004)
Course lecturer in Semiconductor Device Physics, and in CMOS Logic and Memories. Also supervised MPhil research projects.

OTHER ACADEMIC APPOINTMENTS:

1. Fellow and College Lecturer, New Hall, Cambridge (1999 – 2007)
   UG Physics supervisor and UG Tutor (1999 – 2007), College Dean (2004 – 2006).
2. Deputy Director, MPhil in Microelectronics and Semiconductor Physics, University of Cambridge (1999 – 2004)
   Organised laboratory courses and research projects.

EDUCATION:

A. Degrees

1. PhD in Physics, Churchill College, University of Cambridge. Awarded 01/1998.
2. MPhil in Microelectronics Engineering and Semiconductor Physics, Churchill College, 1st in class, University of Cambridge. Awarded 10/1993.
3. BSc in Electrical Engineering, NWFP University of Engineering and Technology, Pakistan, 1st Class Honours, Ranked 2nd overall on class list. Awarded 07/1991.

B. Scholarships

1. University of Cambridge
   PhD: ORS Award (10/1994 to 10/1996), Government of Pakistan S&T Scholarship (10/1993 to 10/1996).
   MPhil: Cambridge Commonwealth Trust ODA Scholarship (10/1992 to 10/1993),
2. NWFP University of Engineering and Technology, Pakistan
   BSc (Eng): WAPDA gold medal for academic performance (1991), Merit Scholarships (1989, 1990).

PUBLICATIONS:

A. Publication statistics:

Total publications (150): Journal: 65, Book (Single Author): 1, Book Chapters: 3, Patent: 1, Conferences: 78, Other: 3
Citations (Google Scholar, Dec. 2023): Citations: 1767, H-Index: 26, i10 index: 48
Most cited publications:

Tan *et al*, J. Appl. Phys. **94**, 633 (2003). Cited 133 times.
Durrani, 'Single-electron devices and circuits in silicon', Imperial College Press (2010). Cited 97 times.
Rafiq *et al*, Appl. Phys. Lett. **87**, 182101 (2005). Cited 88 times.
Most cited paper since 2007:

Durrani, 'Single-electron devices and circuits in silicon' (2010), Imperial College Press, Cited 97 times.
Servati *et al*, Physica E Vol. 38 p 64 (2007). Cited 59 times.
Krali and Durrani, Appl. Phys. Lett. 102, 143102 (2013). Cited 48 times.

B. Journal Papers:

1. 'Dark-field optical fault inspection of ~10 nm scale room- temperature silicon single-electron transistors', W. He, K-L. Chu, F. Abualnaja, M. Jones, and Z. Durrani, Nanotechnology **34**, 505302 (2023).
2. 'Tunable hybrid silicon single-electron transistor–nanoscale field-effect transistor operating at room temperature', F. Abualnaja, Wenkun He, K-L Chu, A. Andreev, M. Jones, Z. Durrani, Appl. Phys. Lett. **122**, 233504 (2023).
3. 'Single particle entropy stability and the temperature-entropy diagram in quantum dot transistors', F. Abualnaja, Wenkun He, A. Andreev, M. Jones, and Z. Durrani, Phys. Rev. Res. **5**, 033025 (2023)
4. 'Room temperature Szilard cycle and entropy exchange at the Landauer limit in a dopant atom double quantum dot silicon transistor', Z. Durrani, F. Abualnaja, and M. Jones, J. Phys. D: Appl. Phys. **55**, 285304 (2022).
5. 'Device fabrication for investigating Maxwell's Demon at room-temperature using double quantum dot transistors in silicon', F. Abualnaja, W. He, M. Jones, Z. Durrani, Micro and Nano Engineering **14**, 100114 (2022).
6. 'Room-temperature measurement of electrostatically-coupled, dopant-atom double quantum dots in point-contact transistors', F. Abualnaja, C. Wang, V-P Veigang-Radulescu, J. Griffiths, A. Andreev, M. Jones, Z. Durrani, Phys. Rev. Appl. **12**, 064050 (2019).
7. 'Room-temperature single dopant atom quantum dot transistors in silicon, formed by field-emission scanning probe lithography', Z. Durrani, M. Jones, F. Abualnaja, C. Wang, M. Kaestner, S. Lenk, C. Lenk, I. W. Rangelow and A. Andreev, J. Appl. Phys. **124**, 144502 (2018).
8. 'Fast turnaround fabrication of silicon point-contact quantum-dot transistors using combined thermal scanning probe lithography and laser writing', C. Rawlings, Y. K. Ryu, M. Rüegg, N. Lassaline, C. Schwemmer, U. Duerig, A. W Knoll, Z. Durrani, C. Wang, D. Liu, and M. E Jones, Nanotechnology **29**, 505302 (2018).
9. 'Nanofabrication by field-emission scanning probe lithography and cryogenic plasma etching', C. Lenk, M. Hofmann, S. Lenk, M. Kaestner, T. Ivanov, Y. Krivoshapkina, D. Nechepurenko, B. Volland, M. Holz, A. Ahmad, A. Reum, C. Wang, M. Jones, Z. Durrani, I. W. Rangelow, Micr. Eng. **192**, 77–82 (2018).

10. ‘Electron transport and room temperature single-electron charging in 10nm scale PtC nanostructures formed by electron beam induced deposition’ Z. A. K. Durrani, M. E. Jones, C. Wang, M. Scotuzzi, and C. W. Hagen, Nanotechnology **28**, 474002 (2017).
11. ‘Excited states and quantum confinement in room temperature few nanometre scale silicon single electron transistors’, Z. Durrani, M. Jones, C. Wang, D, Liu, J, Griffiths, Nanotechnology **28**, 125208 (2017)
12. ‘Pattern-generation and pattern-transfer for single-digit nano devices’ I. W. Rangelow, A. Ahmad, T. Ivanov, M. Kaestner, Y. Krivoshapkina, T. Angelov, S. Lenk, C. Lenk, V. Ishchuk, M. Hofmann, D. Nechepurenko, I. Atanasov, B. Volland, E. Guliyev, Z. Durrani, M. Jones, C. Wang, D. Liu, A. Reum, M. Holz, N. Nikolov, W. Majstrzyk, T. Gotszalk, D. Staaks, S. Dallorto, and D. L. Olynick, J. of Vac.Sci. & Technol. B **34**, 06K202 (2016).
13. ‘Resonant tunnelling features in a suspended silicon nanowire single-hole transistor’ J. Llobet, E. Krali, C. Wang, J. Arbiol, M. E. Jones, F. Pérez-Murano, Z. A. K. Durrani, Appl. Phys. Lett. **107**, 223501 (2015).
14. ‘Single-electron and quantum confinement limits in length-scaled silicon nanowires’, C. Wang, M. E. Jones, Z. A. K. Durrani, Nanotechnology **26**, 305203 (2015).
15. ‘Charge injection and trapping in TiO2 nanoparticles decorated silicon nanowires arrays’, K. Rasool, M. A. Rafiq, M. Ahmad, Z. Imran, S. S. Batool, A. Nazir, Z. A. K. Durrani, and M. M. Hasan, Appl. Phys. Lett. **106**, 073101 (2015).
16. ‘Inelastic electron tunneling spectroscopy for molecular detection’, Y. H. Zadeh and Z. A. K. Durrani, J. Vac. Sci. & Technol. B **32**, 06F601 (2014).
17. ‘Tailoring transport and dielectric properties by surface passivation of silicon nanowires with Polyacrylic acid/TiO_2 nanoparticles composite’, K. Rasool, M. A. Rafiq, Z. A. K. Durrani, Microelectronic Engineering **119**, 141-145 (2014).
18. ‘Seebeck coefficient of one electron’, Z. A. K. Durrani J. Appl. Phys. **115**, 094508 (2014).
19. ‘Seebeck coefficient in silicon nanowire arrays’, E. Krali and Z. A. K. Durrani, Appl. Phys. Lett. **102**, 143102 (2013).
20. ‘Effect of incorporation of zinc sulfide nanoparticles on carrier transport in silicon nanowires’, M. Ahmad, K. Rasool, M.A. Rafiq, M.M. Hasan, C.B. Li, and Z.A.K. Durrani, Physica E **45**, 201 (2012).
21. ‘Enhanced electrical and dielectric properties of polymer covered silicon nanowire arrays’, K. Rasool, M. A. Rafiq, C. B. Li, E. Krali, Z. A. K. Durrani, M. M. Hasan, Appl. Phys. Lett. **101**, 023114 (2012).
22. ‘High ON/OFF ratio and multimode transport in silicon nanochains field effect transistors’, M. A. Rafiq, K. Masubuchi, Z. A. K. Durrani, A. Colli, H. Mizuta, W. I. Milne, S. Oda, Appl. Phys. Lett. **100**, 113108 (2012).
23. ‘Conduction bottleneck in silicon nanochain single electron transistors operating at room temperature’, M. A. Rafiq, K. Masubuchi, Z. A. K. Durrani, A. Colli, H. Mizuta, W. I. Milne, and S. Oda, J. J. Appl. Phys. **51**, 025202 (2012).
24. ‘Schottky-barrier lowering in silicon nanowire field-effect transistors prepared by metal-assisted chemical etching’, M. Zaremba-Tymieniecki and Z.A.K. Durrani, Appl. Phys. Lett. **98**, 102113 (2011).
25. ‘Field-effect transistors using silicon nanowires prepared by electroless chemical etching’, M. Zaremba-Tymieniecki, Chaunbo Li, K. Fobelets, and Z.A.K. Durrani, IEEE Electron Dev. Lett. **31**, 860 (2010).
26. ‘Electrical transport in polymer covered silicon nanowires’. K. Fobelets, P. W. Ding, N. Mohseni Kiasari, and Z. A. K. Durrani, IEEE Trans. Nanotech. **99**, 1 (2010).
27. ‘Electron transport in silicon nanocrystals and nanochains’, Z. A. K. Durrani, and M. A. Rafiq, Micr. Eng. **86**, 456 (2009).
28. ‘Field dependant hopping conduction across silicon nanocrystal films’, M. A. Rafiq, Z. A. K. Durrani, H. Mizuta, M. M. Hassan and S. Oda, J. Appl. Phys. **104**, 123710 (2008).
29. ‘Control of Electrostatic Coupling Observed for Silicon Double Quantum Dot Structures’ G. Yamahata, Y. Tsuchiya, S. Oda, Z. A. K. Durrani, and H. Mizuta, J. J. Appl. Phys. **47**, 4820 (2008).
30. ‘Room temperature single electron charging in single silicon nanochains’, M. A. Rafiq, Z. A. K. Durrani, H. Mizuta, A. Colli, P. Servati, A. C. Ferrari, W. I. Milne, and S. Oda, J. Appl. Phys. **103**, 53705 (2008).
31. ‘Fabrication of vertical nanopillar devices’, M.A. Rafiq, H. Mizuta, Shigeyasu Uno, Z.A.K. Durrani, Micr. Eng. **84**, 1515 (2007).
32. ‘Scalable silicon nanowire photodetectors’, P. Servati, A. Colli, S. Hofmann, Y.Q. Fu, P. Beecher, Z.A.K. Durrani, A.C. Ferrari, A.J. Flewitt, J. Robertson, W.I. Milne, Physica E **38**, 64 (2007).
33. ‘Hopping transport in size-controlled Si nanocrystals’, M. A. Rafiq, Y. Tsuchiya, H. Mizuta, S. Oda, Shigeyasu Uno, Z. A. K. Durrani, W. I. Milne, J. Appl. Phys. **100**, 14303 (2006).
34. ‘Identifying single-electron charging islands in a two-dimensional network of nanocrystalline silicon grains using Coulomb oscillation fingerprints’, M. A. H. Khalafalla, H. Mizuta, Z. A. K. Durrani, Phys. Rev. B, **74**, 35316 (2006).
35. ‘Observation of interdot coupling phenomena in nanocrystalline silicon point-contact structures’, M.A.H. Khalafalla, H. Mizuta, S. Oda, Z.A.K. Durrani, Current Appl. Phys. **6**, 536 (2006).
36. ‘Charge injection and trapping in silicon nanocrystals’, M. A. Rafiq, Y. Tsuchiya, H. Mizuta, S. Oda, S. Uno, Z. A. K. Durrani, W. I. Milne, Appl. Phys. Lett. **87**, 182101 (2005).
37. ‘Inter-grain coupling effects on Coulomb oscillations in dual-gated nanocrystalline silicon point-contact transistors’, M. A. H. Khalafalla, Z. A. K. Durrani, H. Mizuta, H. Ahmed, S. Oda., Thin Solid Films **487**, 255 (2005).
38. ‘Nanosilicon for single-electron devices’, H. Mizuta, Y. Furuta, T. Kamiya, Y.T. Tan, Z.A.K. Durrani, S. Amakawa, K. Nakazato, H. Ahmed, Current Appl. Phys. **4**, 98 (2004).
39. ‘Coherent states in a coupled quantum dot nanocrystalline silicon transistor’, M. A. H. Khalafalla, Z. A. K. Durrani, H. Mizuta, Appl. Phys. Lett. **85**, 2262 (2004).
40. ‘Universal three-way few-electron switch using single-electron transistors’, J. He, Z. A. K. Durrani, H. Ahmed, Appl. Phys. Lett. **85**, 308 (2004).
41. ‘Two-way switch for binary decision diagram logic using silicon single-electron transistors’, J. He, Z. A. K. Durrani, H. Ahmed, Micr. Eng.**73-74**, 712 (2004).
42. ‘Switching of single-electron oscillations in dual-gated nanocrystalline silicon point-contact transistors’, M. A. H. Khalafalla, H. Mizuta, Z. A. K. Durrani, IEEE Trans. Nanoelectronics **2**, 271 (2003).
43. ‘Room temperature nanocrystalline silicon single-electron transistors’, Y. T. Tan, T. Kamiya, Z. A. K. Durrani, H. Ahmed, J. Appl. Phys. **94**, 633 (2003).

44. ‘Single-electron charging phenomena in nano-polycrystalline silicon point contact transistors’, H. Mizuta, Y. Furuta, T. Kamiya, Y. T. Tan, Z. A. K. Durrani, K. Nakazato, H. Ahmed, Solid State Phenomena, **93**, 419 (2003).
45. ‘Silicon single-electron parametron cell for solid-state quantum information processing’, E. G. Emiroglu, Z. A. K. Durrani, D. G. Hasko, D. A. Williams, Micr. Eng. **67-68**, 755 (2003).
46. 'Coulomb blockade, single electron transistors and circuits in silicon', Z. A. K. Durrani, Physica E **17**, 572-578 (2003).
47. ‘Reduction of grain-boundary potential barrier height in polycrystalline silicon with hot H_2O-vapor annealing probed using point-contact devices’, T. Kamiya, Z. A. K. Durrani, H. Ahmed, T. Sameshima, Y. Furuta, H. Mizuta, N. Lloyd, J. Vac. Sci. & Technol B, **21**, 1000 (2003).
48. ‘Control of grain-boundary tunneling barriers in polycrystalline silicon’, T. Kamiya, Z. A. K. Durrani, H. Ahmed, Appl. Phys. Lett. **81**, 2388 (2002).
49. ‘Single-electron charging in nanocrystalline silicon point-contacts’, Z. A. K. Durrani, T. Kamiya, Y. T. Tan, H. Ahmed, Micr. Eng. **63**, 267 (2002).
50. ‘Modification of the tunneling barrier in a nanocrystalline silicon single-electron transistor’, T. Kamiya, Y. T. Tan, Z. A. K. Durrani, H. Ahmed, J. Non-Cryst. Solids, **299-302**, 405 (2002).
51. ‘Characterisation of tunnel-barriers in polycrystalline silicon point-contact single-electron transistors’, Y. Furuta, H. Mizuta, K. Nakazato, T. Kamiya, Y. T. Tan, Z. A. K. Durrani, K. Taniguchi, J. J Appl Phys. **41**, 2675 (2002).
52. ‘Single-electron parametron memory cell’, E. G. Emiroglu, Z. A. K. Durrani, D. G. Hasko, D. A. Williams, J. Vac. Sci. &Technol. B, **20**, 2806 (2002).
53. ‘Growth, structure, and transport properties of thin (>10 nm) *n*-type microcrystalline silicon prepared on silicon oxide and its application to single-electron transistor’, T. Kamiya, K. Nakahata, Y. T. Tan, Z. A. K. Durrani, I. Shimuzu, J. Appl. Phys. **89**, 6265 (2001).
54. ‘Nanoscale Coulomb blockade memory and logic devices’, H. Mizuta, H-O Muller, K. Tsukagoshi, D. Williams, Z. Durrani, A. Irvice, G. Evans, S. Amakawa, K. Nakazato, H. Ahmed, Nanotechnology **12**, 155 (2001).
55. ‘Carrier transport across a few grain boundaries in highly doped polycrystalline silicon’, Y. Furuta, H. Mizuta, K. Nakazato, Y. T. Tan, T. Kamiya, Z. A. K. Durrani, H. Ahmed, K. Taniguchi, J. J. Appl. Phys. **40**, L615-L617 (2001).
56. ‘Single-electron effects in side-gated point contacts fabricated in low-temperature deposited nanocrystalline silicon films’, Y. T. Tan, T. Kamiya, Z. A. K. Durrani, H. Ahmed, Appl. Phys. Lett. **78**, 1083 (2001).
57. ‘Electrical and structural properties of solid phase crystallised polycrystalline silicon and their correlation to single-electron effects’, Y. T. Tan, Z. A. K. Durrani, H. Ahmed, J. Appl. Phys. **89**, 1262 (2001).
58. ‘Coulomb blockade memory using integrated single-electron transistor / metal-oxide-semiconductor transistor gain cells’, Z. A. K. Durrani, A. C. Irvine, H. Ahmed, IEEE Trans. Elec. Dev. **47**, 2334 (2000).
59. ‘A high-speed silicon based few-electron memory with metal-oxide-semiconductor field-effect transistor gain element’, A. C. Irvine, Z. A. K. Durrani, H. Ahmed, J. Appl. Phys. **87**, 8594 (2000).
60. ‘Simulating Si multiple tunnel junctions from pinch-off to ohmic conductance’, H.-O. Muller, D. A. Williams, H. Mizuta, Z. A. K. Durrani, Mat. Sci. & Eng. B, **74**, 36 (2000).
61. ‘Simulation of Si multiple tunnel junctions’, H.-O. Muller, D. A. Williams, H. Mizuta, Z. A. K. Durrani, A. C. Irvine, H. Ahmed, Physica B, **272**, 85 (1999).
62. ‘A memory cell with single-electron and metal-oxide-semiconductor transistor integration’, Z. A. K. Durrani, A. C. Irvine, H. Ahmed, K. Nakazato, Appl. Phys. Lett. **74**, 1293 (1999).
63. ‘Single-electron effects in heavily doped polycrystalline silicon nanowires’, A. C. Irvine, Z. A. K. Durrani, H. Ahmed, S. Biesemans, Appl. Phys. Lettl. **73**, 1113 (1998).
64. ‘Field enhanced blockade of the confined energy levels in nanometer scale pillar arrays’, B. W. Alphenaar, Z. A. K. Durrani, M. Wagner, K. Kohler, Surface Sci. **362**, 185 (1996).
65. ‘Resistance bi-stability in resonant tunnelling diode pillar arrays’, B. W. Alphenaar, Z. A. K. Durrani, A. P. Herbele, M. Wagner, Appl. Phys. Lett. **66**, 1234 (1995).

C. Book:

1. ‘Single-electron devices and circuits in silicon’
   Z. A. K. Durrani
   Imperial College Press, 285 pages, London (2010)

D. Book chapters:

1. 'Nanosilicon single-electron transistors and memory', Z A K Durrani and H Ahmed, in ‘Nanosilicon’, Ed. V. Kumar, Elsevier Press (2007).
2. ‘Electron Transport in Nanocrystalline Silicon’, Z. A. K. Durrani, T. Kamiya, H. Mizuta, in Recent Research Developments in Applied Physics (Vol. 7), Transworld Research Network, (2004).
3. ‘Charge gating of nanometer scale pillar arrays’, Z. A. K. Durrani, B. W. Alphenaar, K. Kohler, in ‘Hot Carriers in Semiconductors’ p283, Plenum Press (1996) (Peer Reviewed Proceeding)

E. Patent:

1. GaAs nano-pillar memory device:
   U. S. Patent Number 5,811,832 (Filed Oct. 1996, Issued Sept. 1998).

F. Other publications:

1. ‘Semiconductor Industry in the U.K.’
   Zahid Durrani and Mervyn Jones, (2022), Submission to the House of Commons Business, Energy and Industrial Strategy Committee. Submission available online on the HoC website:
   https://committees.parliament.uk/writtenevidence/109129/html/
2. ‘Scanning probe lithography for electronics at the 5nm scale’
   Zahid Durrani, Marcus Kaestner, Manuel Hofer, Tzvetan Ivanov and Ivo Rangelow, SPIE Newsroom, 19 Feb. (2013).

3. ‘Electrifying possibilities’, Zahid Durrani, Business Technology Supplement, Guardian and Daily Telegraph, UK 30 Nov. (2012)

G. Conference papers:

Invited Talks (17) indicated in ‘Bold’.

1. ‘Conventional Fabrication Techniques with High Yield for a Tuneable Room Temperature Single-electron Transistor and Field-effect Transistor’, Kai-Lin Chu, Faris Abualnaja, Wenkun He, Mervyn Jones, Zahid Durrani, Oral presentation, Micro and Nano Engineering (MNE) 2023, Berlin, Sept, 2023.
2. ‘Quantum Szilard cycle and information-entropy exchange in a room-temperature dopant atom double quantum dot transistor’, F. Abualnaja, A. Andreev, Jonathan Griffiths, M. Jones, Z. Durrani 2022 Silicon Quantum Electronics Workshop, Orford, Quebec, Oct. 2022.
3. ‘Dark-field optical fault detection for point-contact single electron transistors’, W. He, K-L Chu, F. Abualnaja, M. E. Jones, Z. A K Durrani, Oral presentation, at Micro and Nano Engineering (MNE) 2022, Brussels, Sept, 2022
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